

Change History

Voltage Rails		ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT		X	X	X	X	
3V_591		X	X	X	X	
5VPCU		X	X	X	X	
+3V_S5		X	X	X	X	S5_ON
3V_LAN		X	X	X	X	
+1.5V_S5		X	X	X	X	S5_ON
+1.8VSUS		X	X			SUS_ON
+3VSUS		X	X			SUS_D
+5VSUS		X	X			SUS_D
SMDDDR_VTERM	DDR Termination voltage	X	X			MAINON
SMDDDR_VREF		X				MAINON
VGA_PCIE_1.2V		X				MAINON
VCC_CORE	Core voltage for Processor	X				VR_ON
+VCCP	1.05V rail for Processor I/O	X				MAINON
+1.5V		X				MAINON
+1.8V		X				MAIND
+2.5V		X				MAIND
+3V		X				MAIND
+5V						MAIND
+12V		X				MAINON
+3VRUN		X				PCI Switch Power ON
+5VRUN		X				PCI Switch Power ON

5/28

- 1.System DVI DET function move in EZ port , So Del Q47,R557
 - 2.Addition AND gate for DOCKING Power Good AND DockingIN Singal combine Circuit
 - 3.Addition Power led circuit for system
 - 4.Change D34 AND D35 + -
 - 5.Addition LID Switch and LID connector
 - 6.Addition RC Delay for PCIE1.2V
 - 7.Change EC Three GPIO port same to ZL2
- 5/31
- 1.Change C145 PCB Footprint to 3528
 - 2.Combine USB and bluetooth connector to 19pin connector 87212-1900
 - 3.Change PCBFootprint 88216-1200 to 88213-1200
 - 4.Change USB connector bypass C1 to 0805 10u
 - 5.Adjust 80pin connector 3 singal
- 6/1
- 1.Update power all circuit for GND name
 - 2.Addition OR to PRST
 - 3.Change IDE RST
- 6/2
- 1.Change ICH-6 USB Port
 - 2.Del CDR,CDL,CDGND Singal and DEL prevent CDR,CDL,CDGND noise circuit
- 6/4
- 1.U49_U50, Form 3VRUN change to +3V AND CHANGE MINPCI connector to PCI BUS,And addition PCI SWRST # AND PCI SWRST1#
 - 2.Change BT POWER NAME
 - 3.Change VOIP AGND
- 6/7
- 1.Change VOIP AGND TO AGND2 for Layout

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+Smart Card	AD25	1	PIRQC/B
Mini-PCI	AD19	2	PIROB/D
LAN	AD22	0	PIROA
1394	AD23	3	PIROD

EC SM Bus1 address

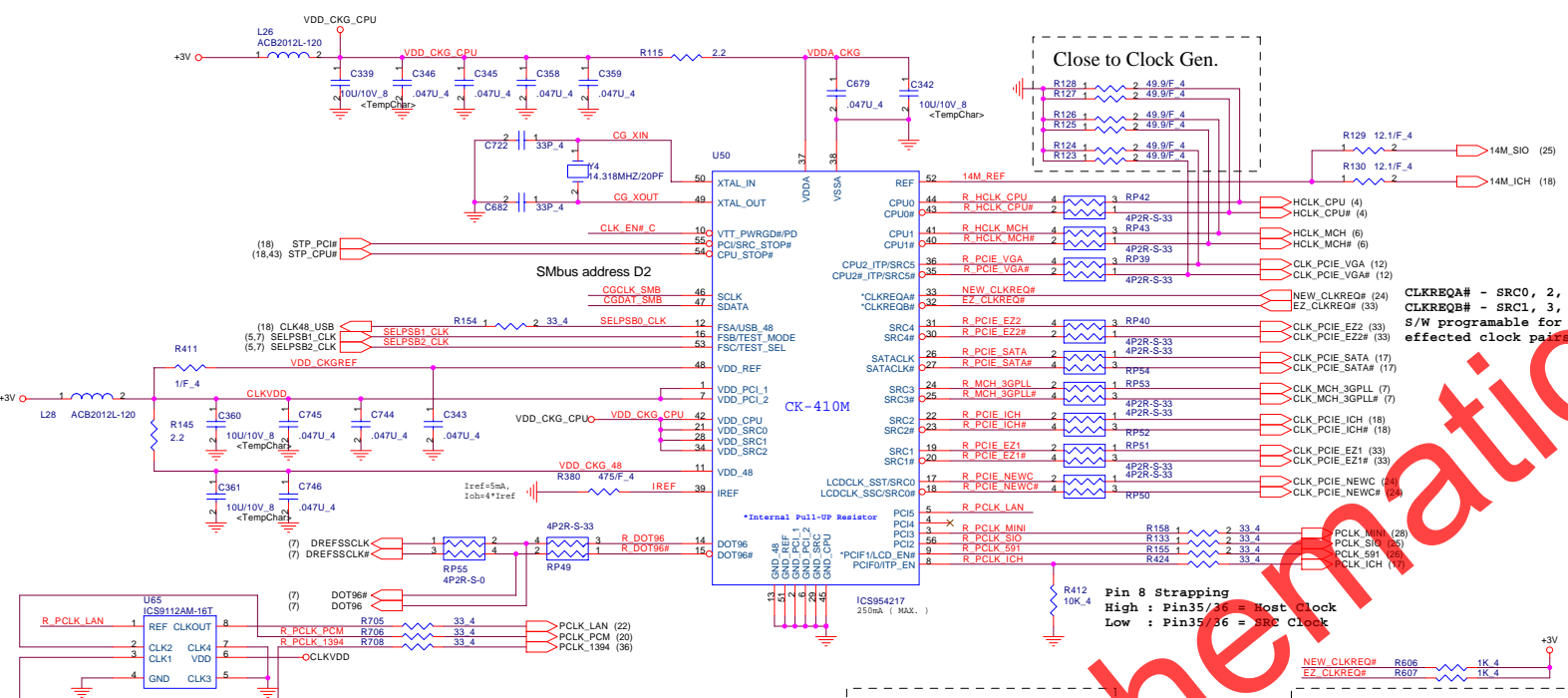
Device

Smart Battery
THERMAL SENSOR
LIGHT SENER
VOIP FLASH ROM

ICH6-M SM Bus address

Device

SODIMM	1010 000X b
Clock Gen	1101 001x b



Resistor Stuff Table

	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X

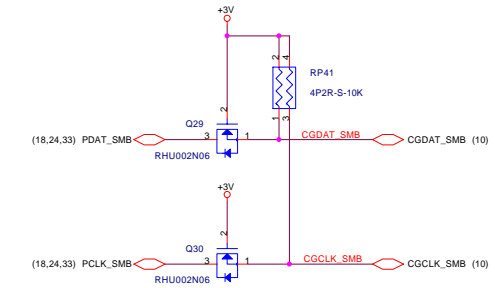
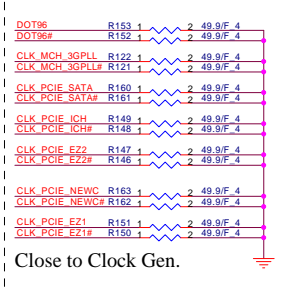
Clock Gen. Frequency Selection Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

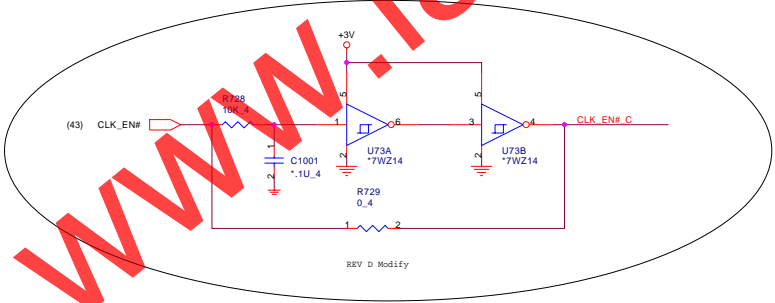
DOTHAN BSEL Output Value

FSB Frequency	DOTHAN A-Step BSEL1	DOTHAN A-Step BSEL0	DOTHAN B-Step BSEL1	DOTHAN B-Step BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0

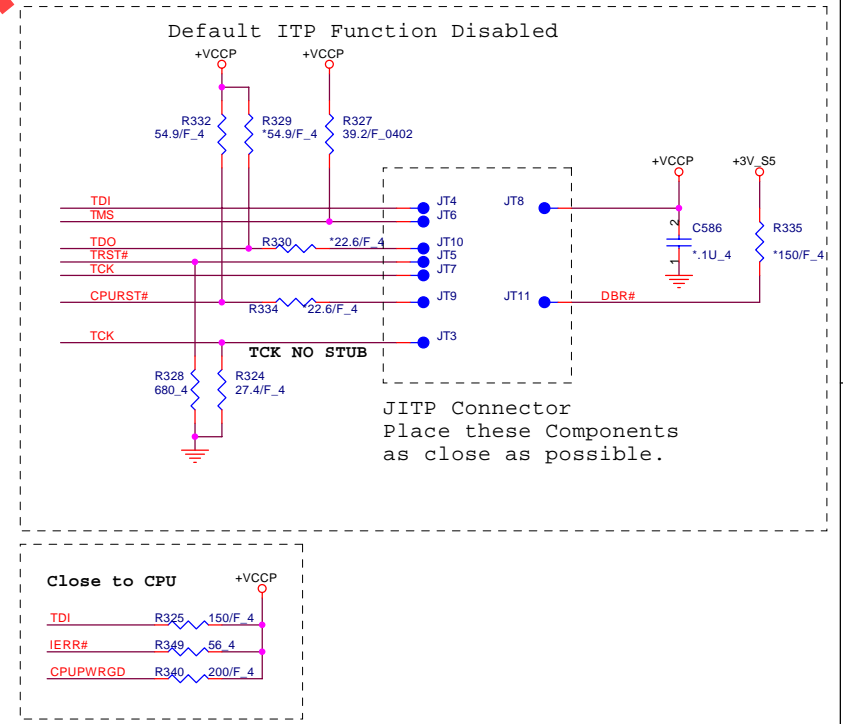
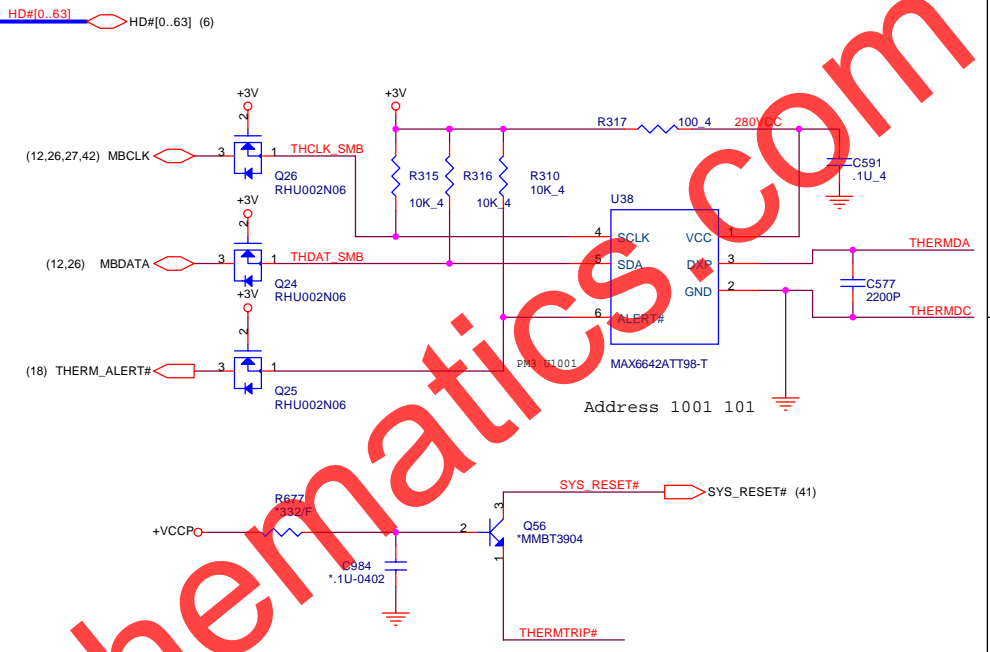
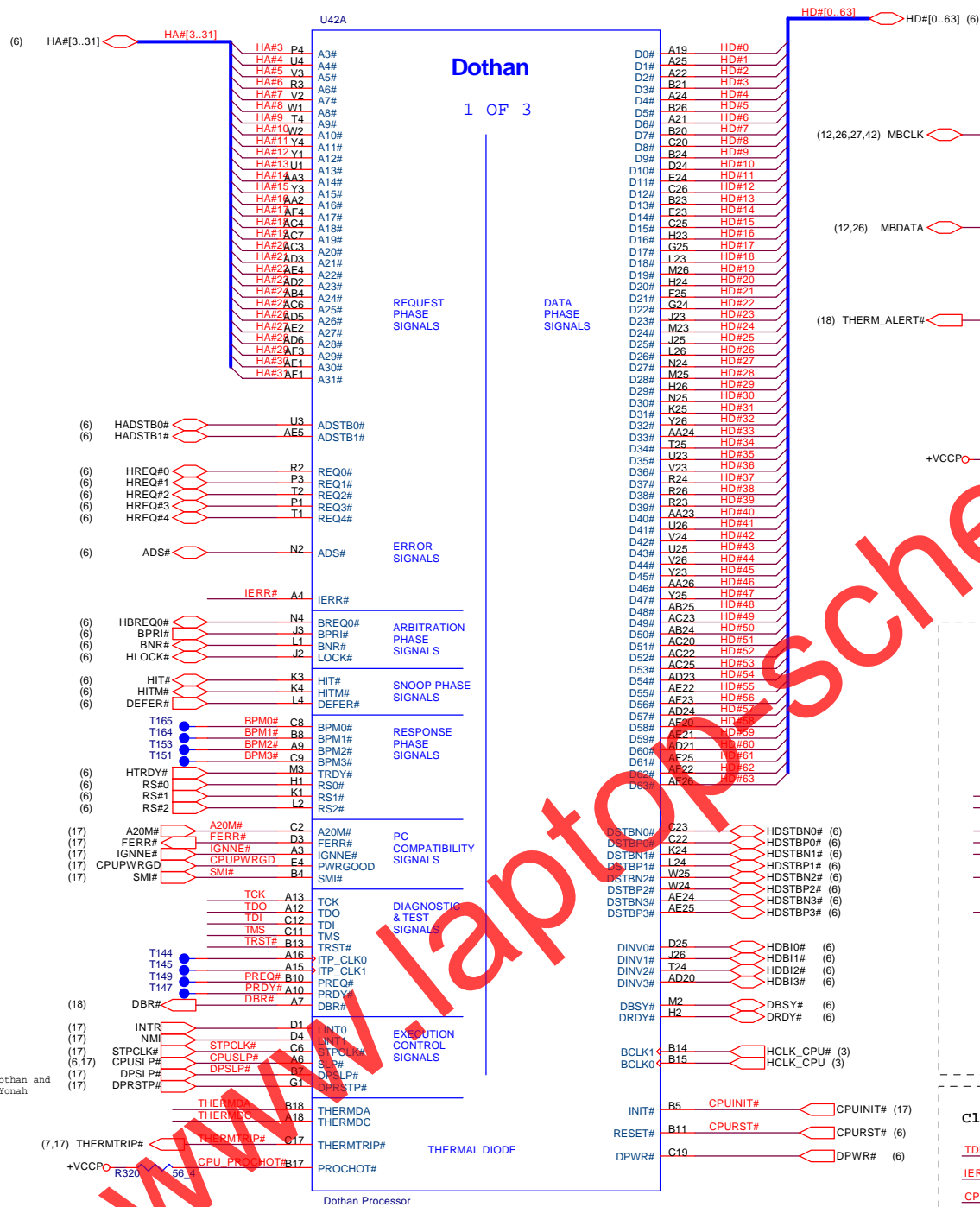
Close to Clock Gen.

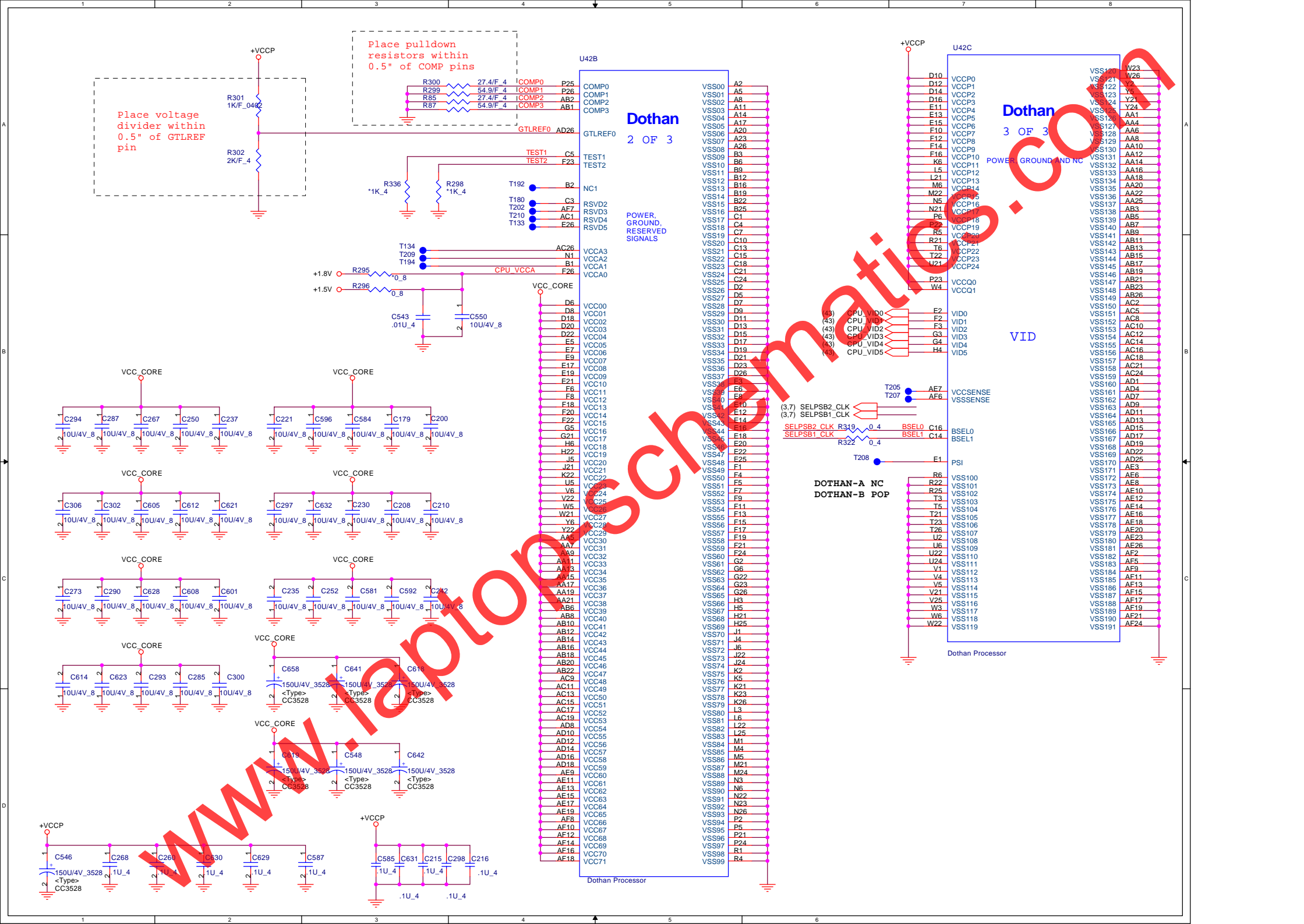


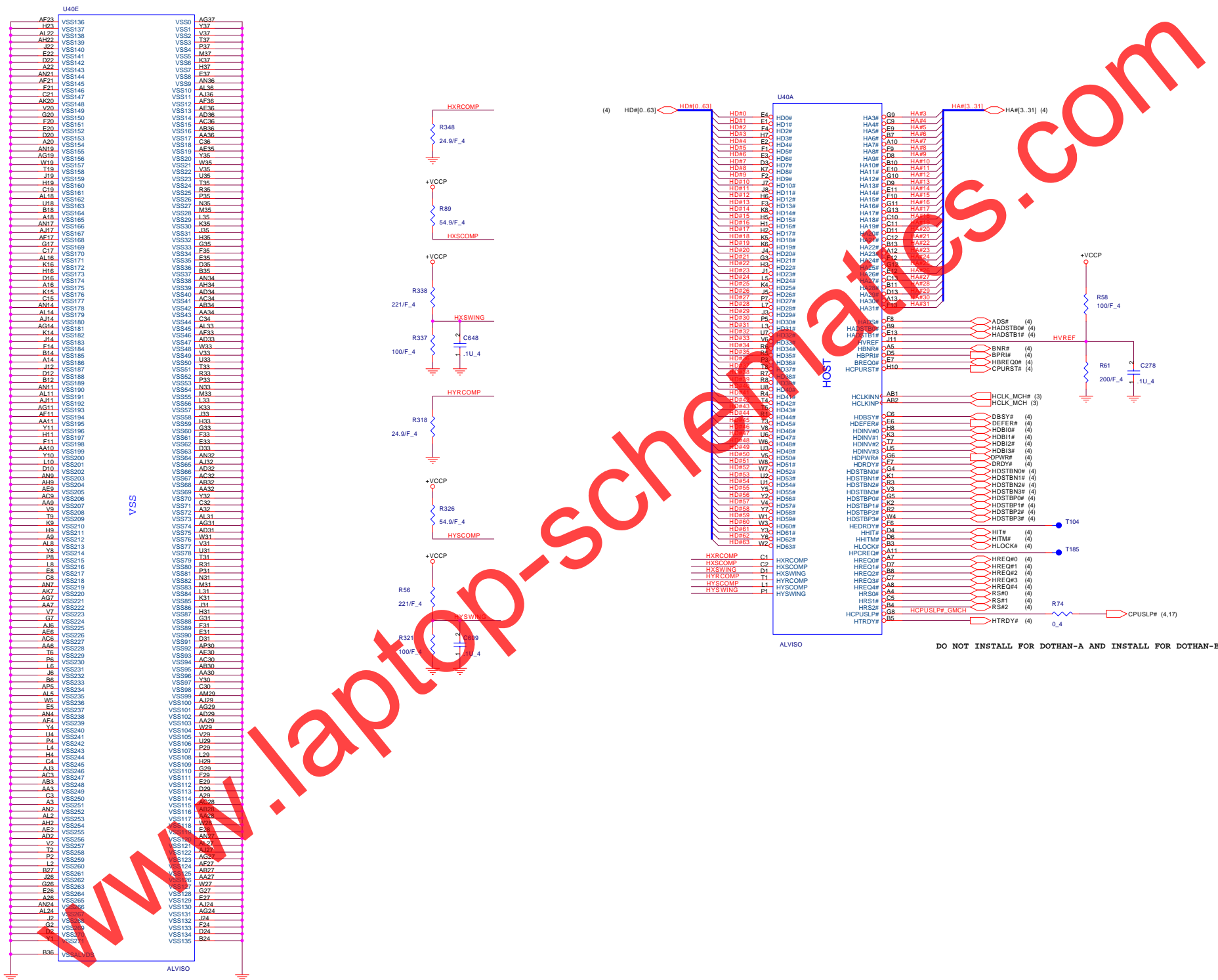
These are for backdrive issue

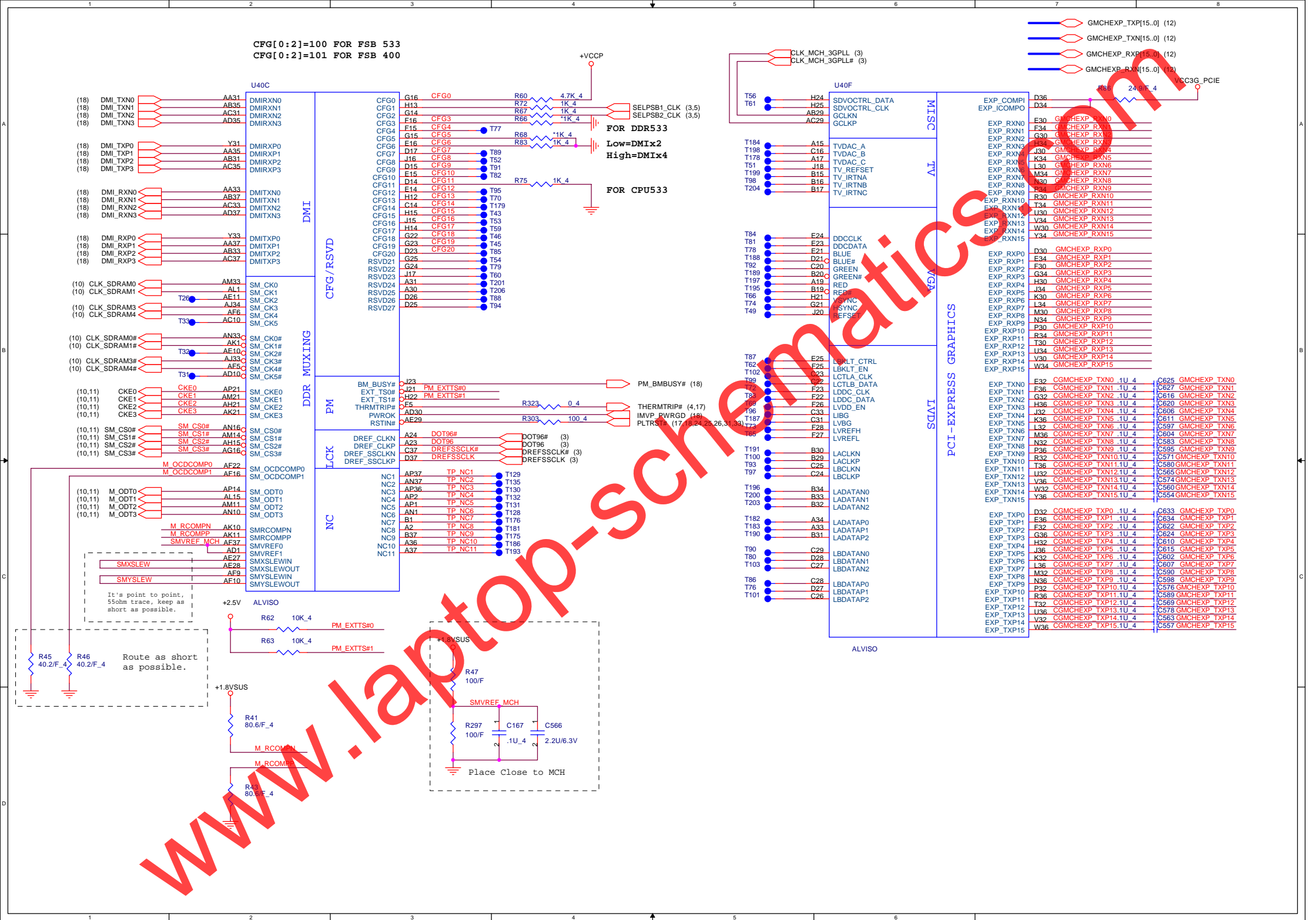


REV D Modify

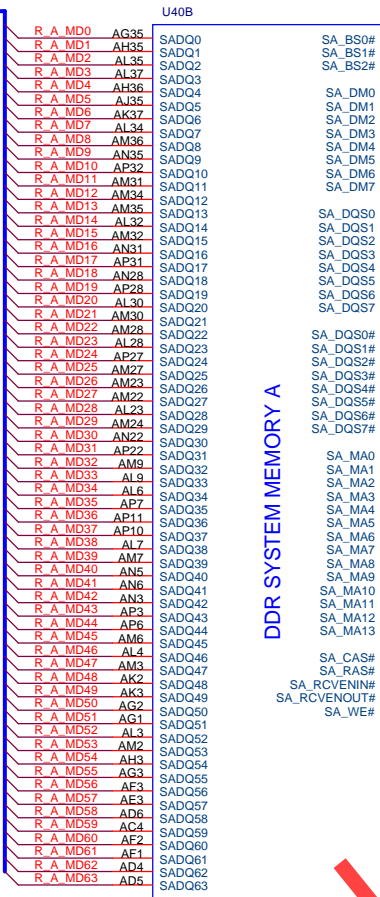




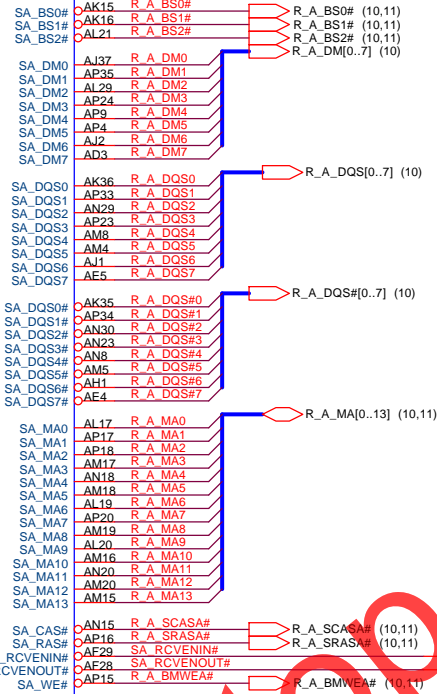




(10) R_A_MD[0..63]



DDR SYSTEM MEMORY A

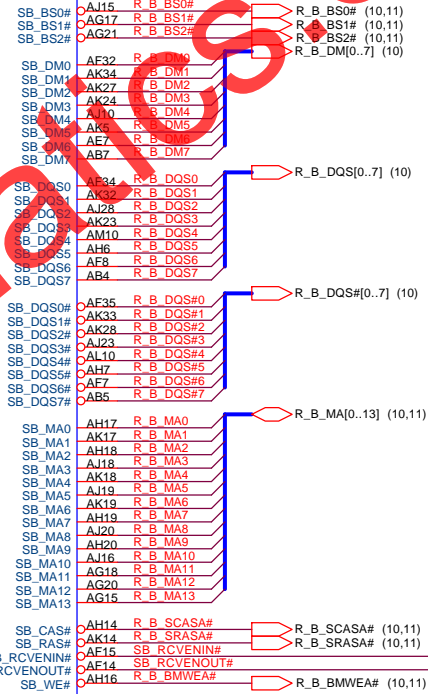


ALVISO

(10) R_B_MD[0..63]

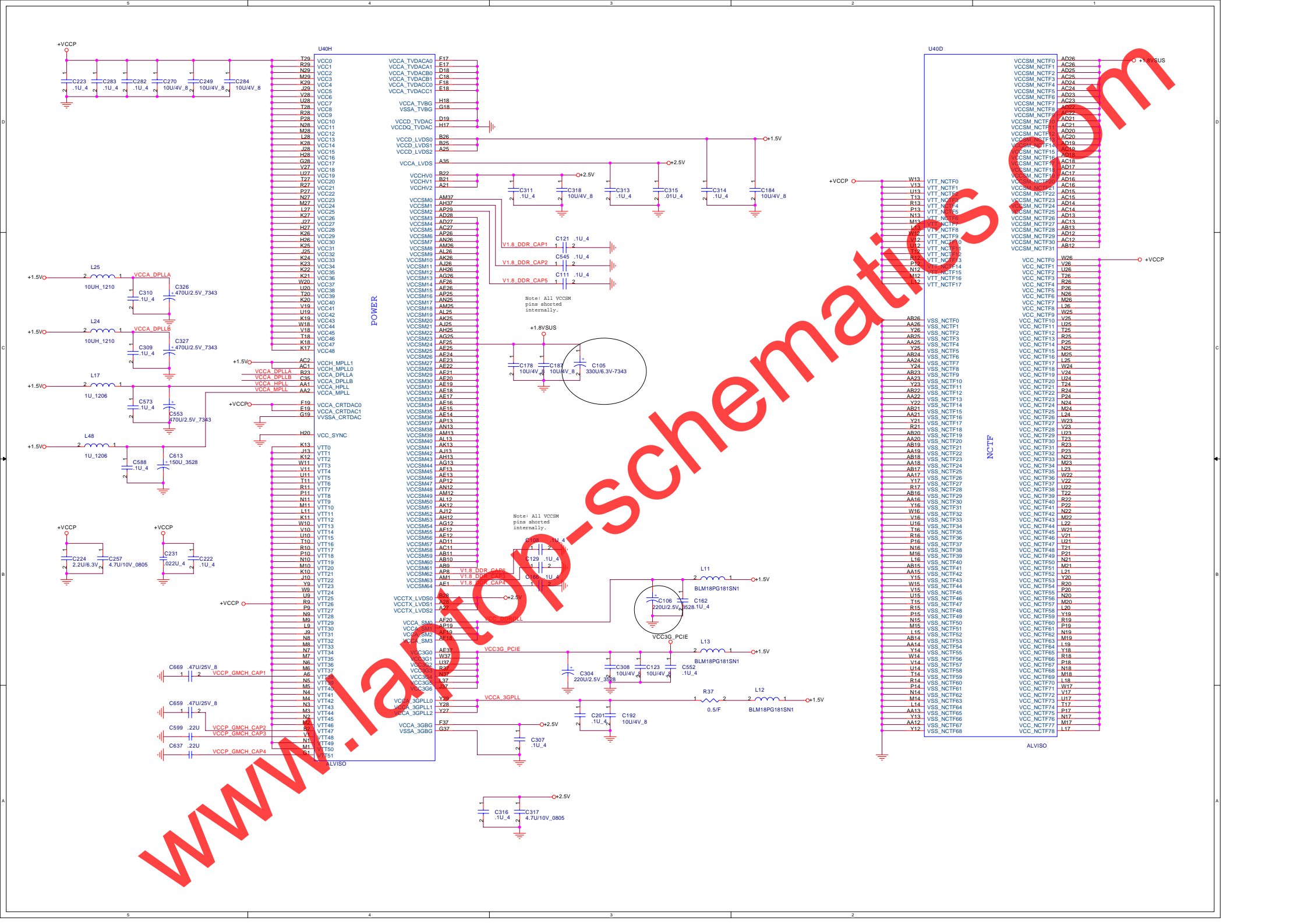


DDR SYSTEM MEMORY B

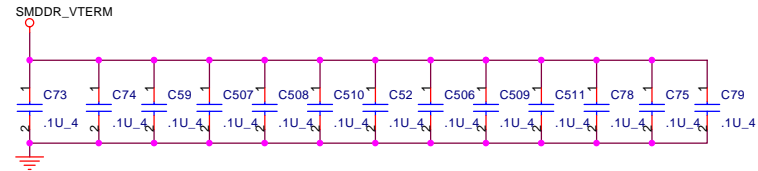


ALVISO

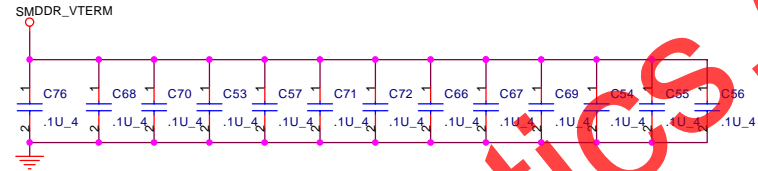
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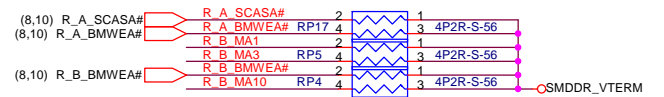
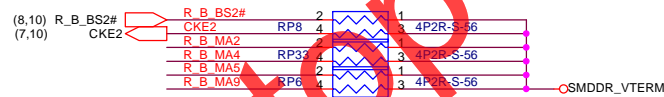
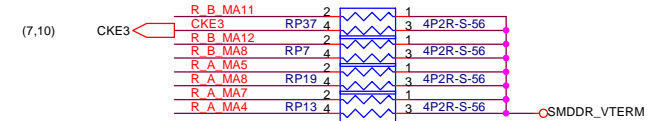
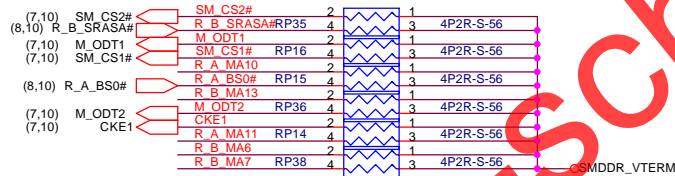
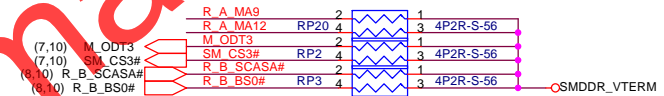
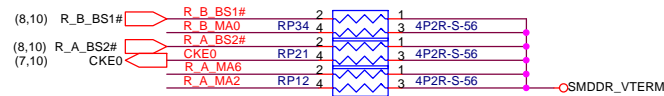




Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



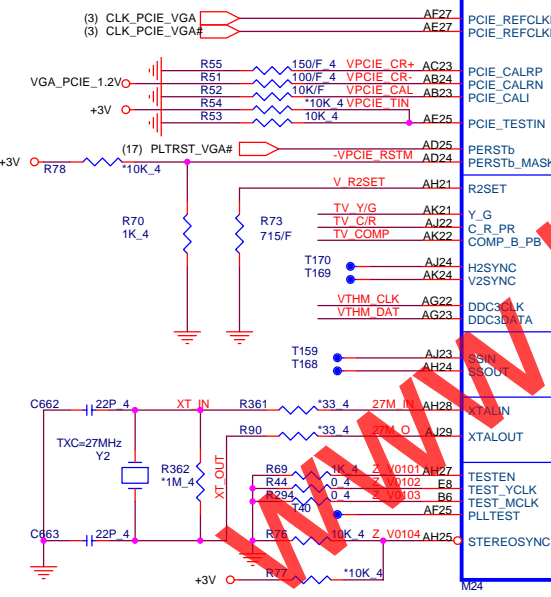
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

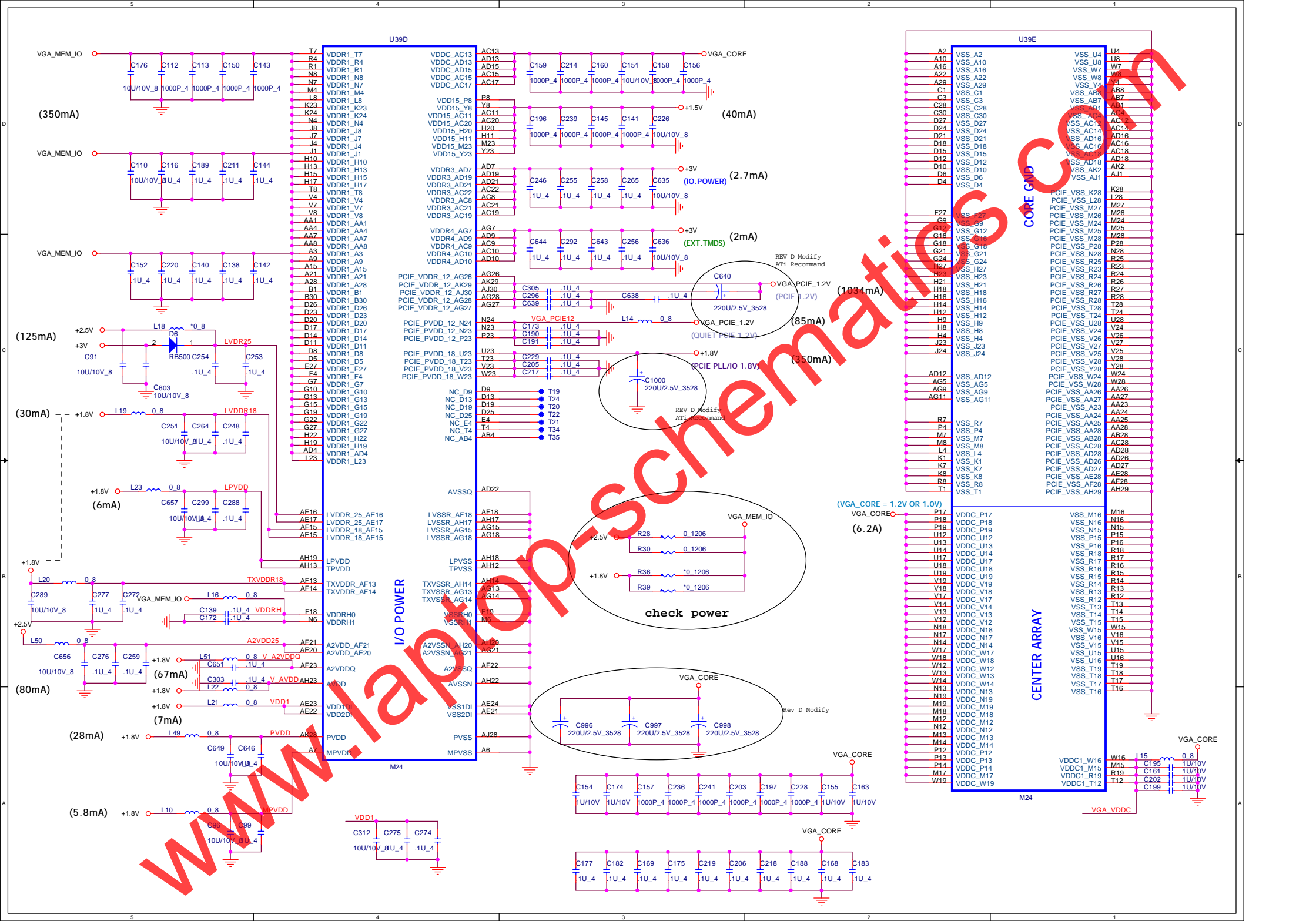


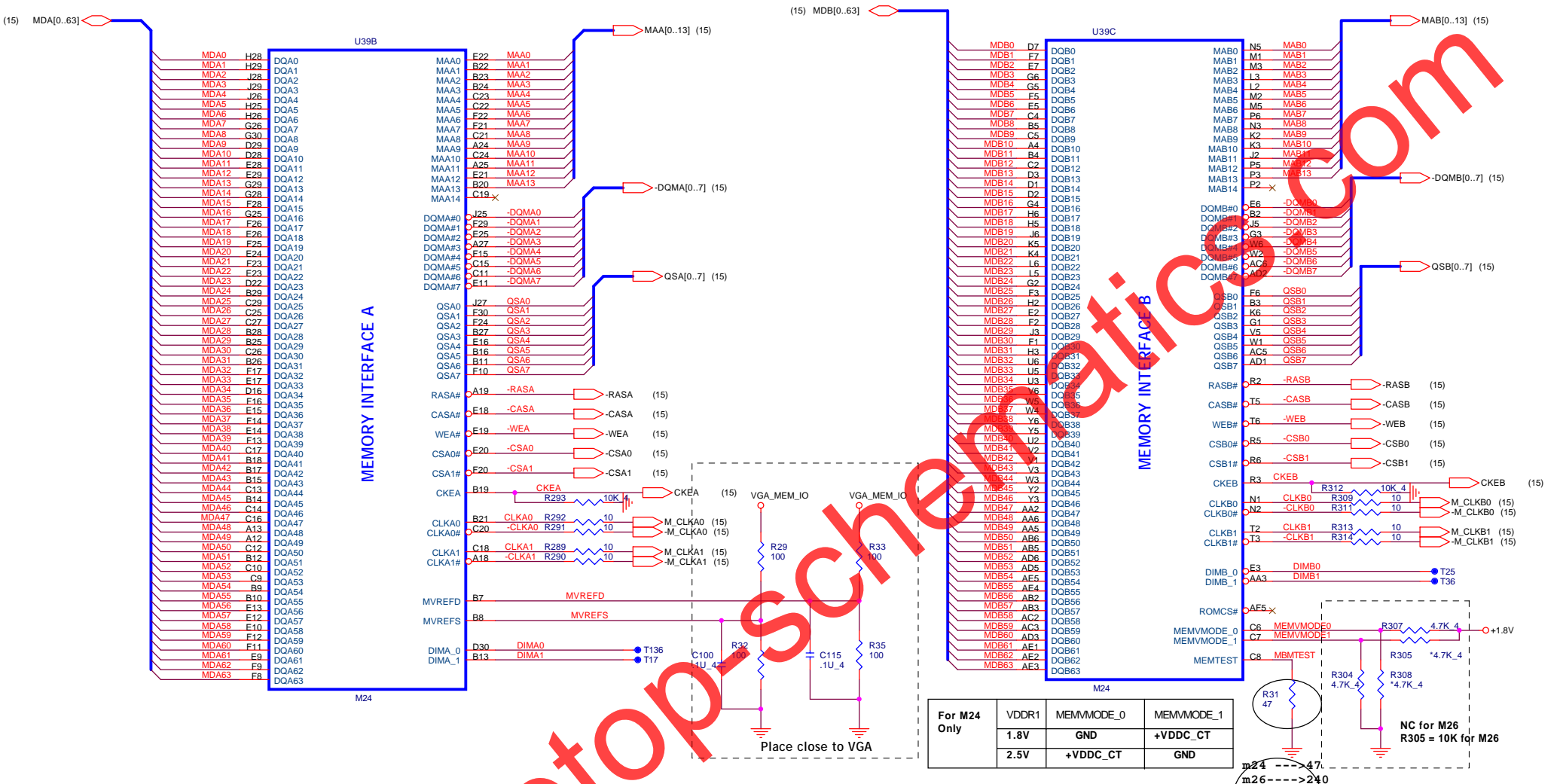
(7) GMCHEXP_TXP[0..15]
(7) GMCHEXP_TXN[0..15]
(7) GMCHEXP_RXP[0..15]
(7) GMCHEXP_RXN[0..15]

GMCHEXP_TXP0	AH30	PCIE_RX0P
GMCHEXP_TXN0	AG30	PCIE_RX0N
GMCHEXP_TXP1	AG29	PCIE_RX1P
GMCHEXP_TXN1	AE29	PCIE_RX1N
GMCHEXP_TXP2	AE29	PCIE_RX2P
GMCHEXP_TXN2	AE30	PCIE_RX2N
GMCHEXP_TXP3	AD30	PCIE_RX3P
GMCHEXP_TXN3	AD29	PCIE_RX3N
GMCHEXP_TXP4	AC29	PCIE_RX4P
GMCHEXP_TXN4	AB29	PCIE_RX4N
GMCHEXP_TXP5	AB30	PCIE_RX5P
GMCHEXP_TXN5	AA30	PCIE_RX5N
GMCHEXP_TXP6	AA29	PCIE_RX6P
GMCHEXP_TXN6	Y29	PCIE_RX6N
GMCHEXP_TXP7	W29	PCIE_RX7P
GMCHEXP_TXN7	W30	PCIE_RX7N
GMCHEXP_TXP8	V30	PCIE_RX8P
GMCHEXP_TXN8	V29	PCIE_RX8N
GMCHEXP_TXP9	U29	PCIE_RX9P
GMCHEXP_TXN9	T29	PCIE_RX9N
GMCHEXP_TXP10	T30	PCIE_RX10P
GMCHEXP_TXN10	R30	PCIE_RX10N
GMCHEXP_TXP11	R29	PCIE_RX11P
GMCHEXP_TXN11	P29	PCIE_RX11N
GMCHEXP_TXP12	N29	PCIE_RX12P
GMCHEXP_TXN12	N30	PCIE_RX12N
GMCHEXP_TXP13	M30	PCIE_RX13P
GMCHEXP_TXN13	M29	PCIE_RX13N
GMCHEXP_TXP14	L29	PCIE_RX14P
GMCHEXP_TXN14	K29	PCIE_RX14N
GMCHEXP_TXP15	K30	PCIE_RX15P
GMCHEXP_TXN15	J30	PCIE_RX15N

GMCHEXP_RXP0	C301	1U 4	V	GMCHEXP_RXP0	AE26	PCIE_TX0P
GMCHEXP_RXN0	C295	1U 4	V	GMCHEXP_RXN0	AE26	PCIE_TX0N
GMCHEXP_RXP1	C291	1U 4	V	GMCHEXP_RXP1	AC25	PCIE_TX1P
GMCHEXP_RXN1	C286	1U 4	V	GMCHEXP_RXN1	AB25	PCIE_TX1N
GMCHEXP_RXP2	C269	1U 4	V	GMCHEXP_RXP2	AC27	PCIE_TX2P
GMCHEXP_RXN2	C263	1U 4	V	GMCHEXP_RXN2	AB27	PCIE_TX2N
GMCHEXP_RXP3	C271	1U 4	V	GMCHEXP_RXP3	AC26	PCIE_TX3P
GMCHEXP_RXN3	C266	1U 4	V	GMCHEXP_RXN3	AB26	PCIE_TX3N
GMCHEXP_RXP4	C243	1U 4	V	GMCHEXP_RXP4	Y25	PCIE_TX4P
GMCHEXP_RXN4	C238	1U 4	V	GMCHEXP_RXN4	W25	PCIE_TX4N
GMCHEXP_RXP5	C247	1U 4	V	GMCHEXP_RXP5	Y27	PCIE_TX5P
GMCHEXP_RXN5	C240	1U 4	V	GMCHEXP_RXN5	W27	PCIE_TX5N
GMCHEXP_RXP6	C225	1U 4	V	GMCHEXP_RXP6	Y26	PCIE_TX6P
GMCHEXP_RXN6	C209	1U 4	V	GMCHEXP_RXN6	W26	PCIE_TX6N
GMCHEXP_RXP7	C227	1U 4	V	GMCHEXP_RXP7	Y25	PCIE_TX7P
GMCHEXP_RXN7	C213	1U 4	V	GMCHEXP_RXN7	T25	PCIE_TX7N
GMCHEXP_RXP8	C193	1U 4	V	GMCHEXP_RXP8	T27	PCIE_TX8P
GMCHEXP_RXN8	C180	1U 4	V	GMCHEXP_RXN8	T27	PCIE_TX8N
GMCHEXP_RXP9	C194	1U 4	V	GMCHEXP_RXP9	U26	PCIE_TX9P
GMCHEXP_RXN9	C185	1U 4	V	GMCHEXP_RXN9	T26	PCIE_TX9N
GMCHEXP_RXP10	C170	1U 4	V	GMCHEXP_RXP10	P25	PCIE_TX10P
GMCHEXP_RXN10	C164	1U 4	V	GMCHEXP_RXN10	N25	PCIE_TX10N
GMCHEXP_RXP11	C171	1U 4	V	GMCHEXP_RXP11	P27	PCIE_TX11P
GMCHEXP_RXN11	C165	1U 4	V	GMCHEXP_RXN11	N27	PCIE_TX11N
GMCHEXP_RXP12	C148	1U 4	V	GMCHEXP_RXP12	P26	PCIE_TX12P
GMCHEXP_RXN12	C146	1U 4	V	GMCHEXP_RXN12	N26	PCIE_TX12N
GMCHEXP_RXP13	C149	1U 4	V	GMCHEXP_RXP13	L25	PCIE_TX13P
GMCHEXP_RXN13	C147	1U 4	V	GMCHEXP_RXN13	L25	PCIE_TX13N
GMCHEXP_RXP14	C134	1U 4	V	GMCHEXP_RXP14	L27	PCIE_TX14P
GMCHEXP_RXN14	C132	1U 4	V	GMCHEXP_RXN14	K27	PCIE_TX14N
GMCHEXP_RXP15	C137	1U 4	V	GMCHEXP_RXP15	L26	PCIE_TX15P
GMCHEXP_RXN15	C133	1U 4	V	GMCHEXP_RXN15	K26	PCIE_TX15N

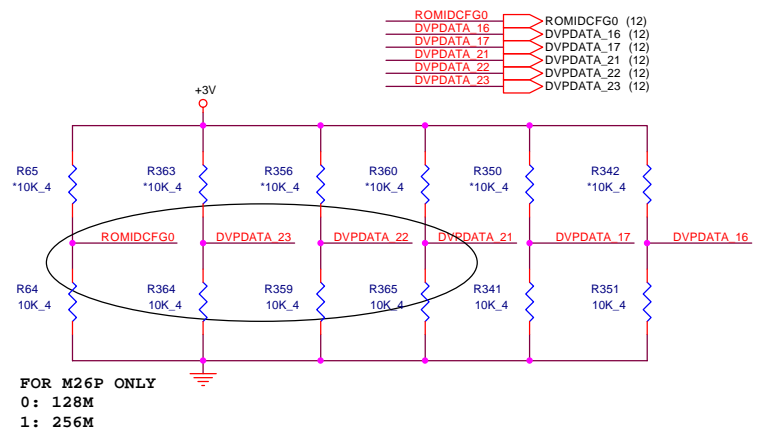


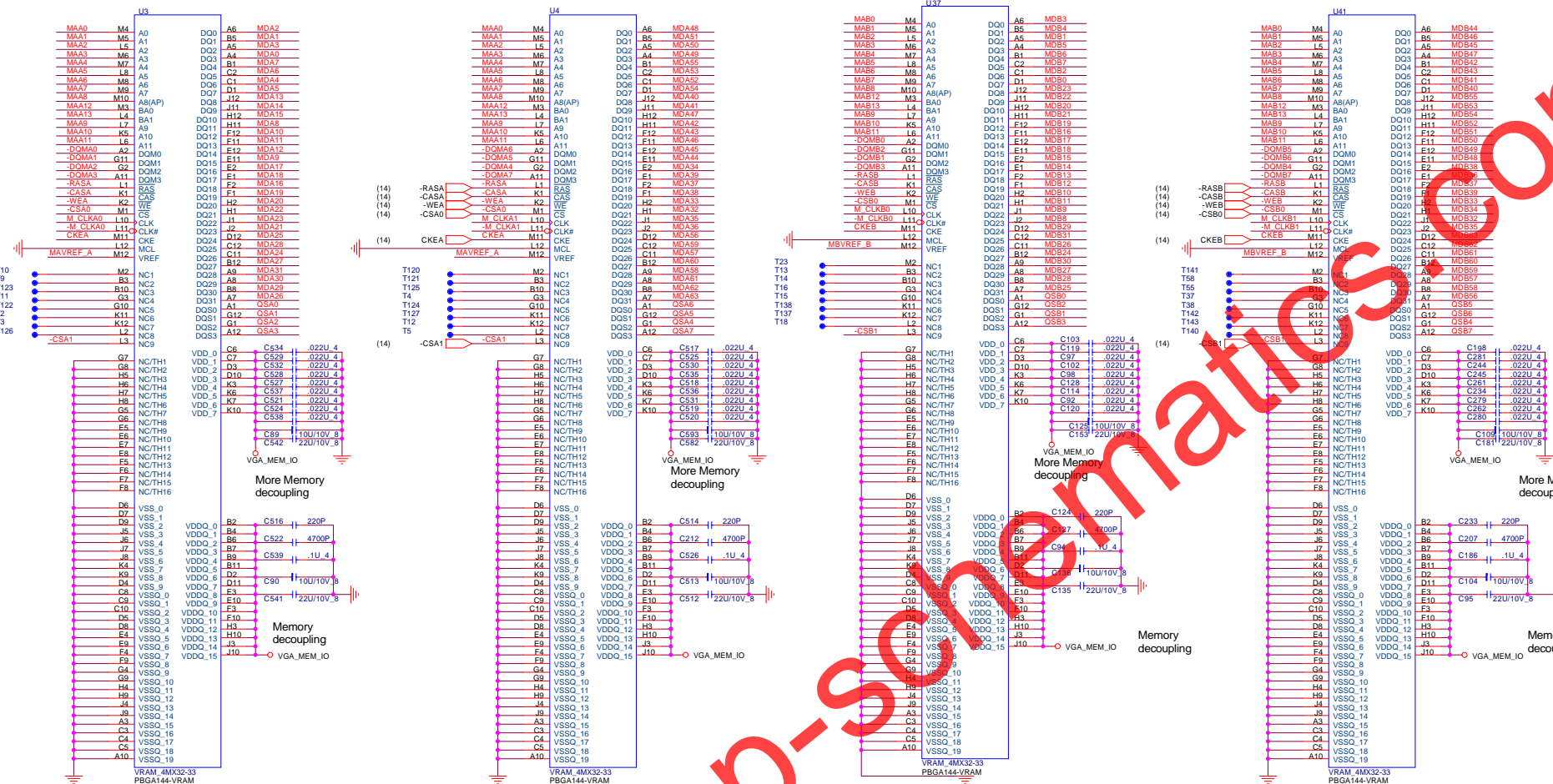




STRAPS PIN

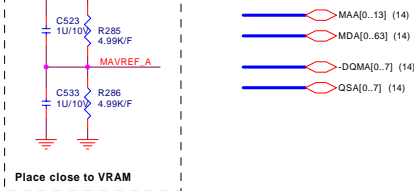
GPIO(9,13:11) INT P/D	ROMIDCFG
	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21-23 MEM TYPE	DVPDATA_21: 0-4Mx32 1=8Mx32 DVPDATA_22: 0-128M 1=64M DVPDATA_23: 0-Hynix 1-Samsung





VGA DDR MEMORY A

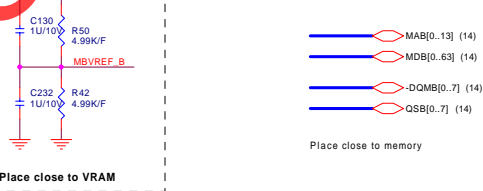
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA



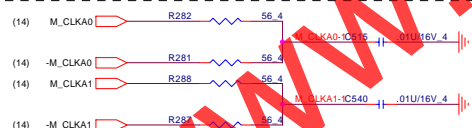
Place close to VRAM

VGA DDR MEMORY B

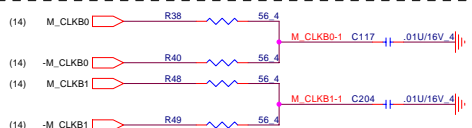
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA



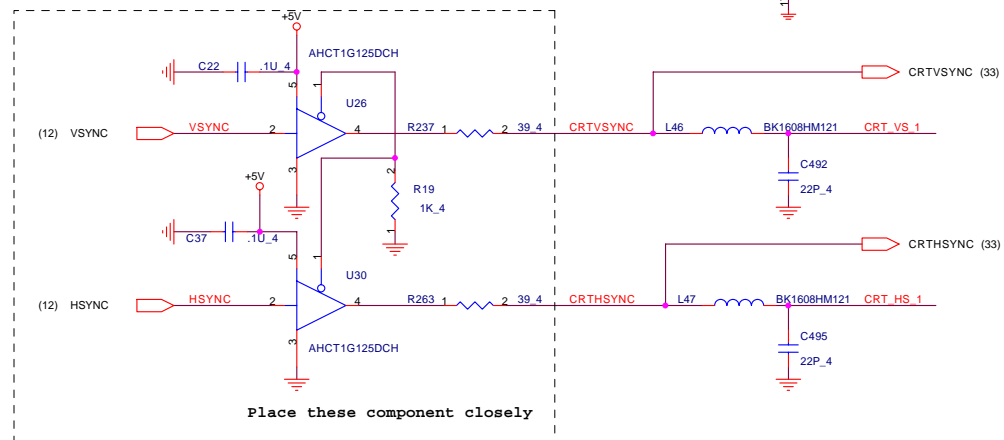
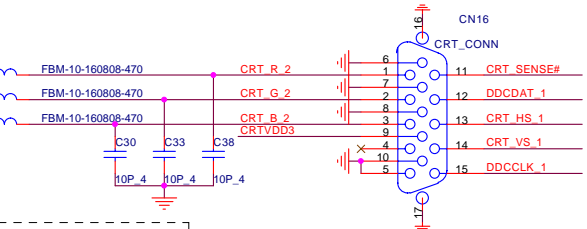
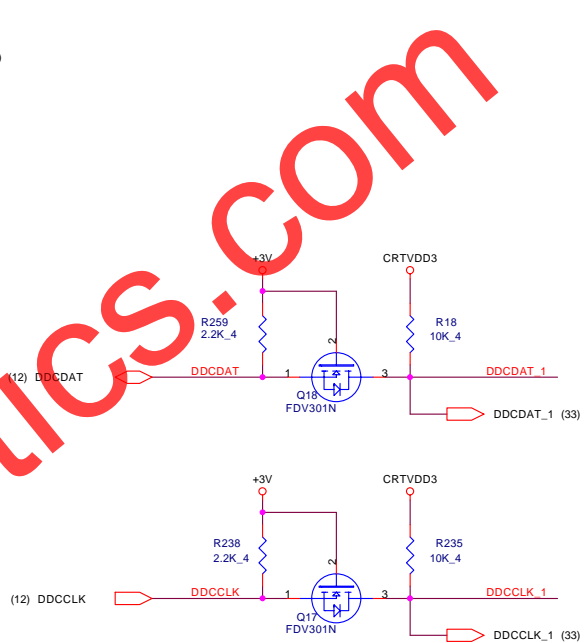
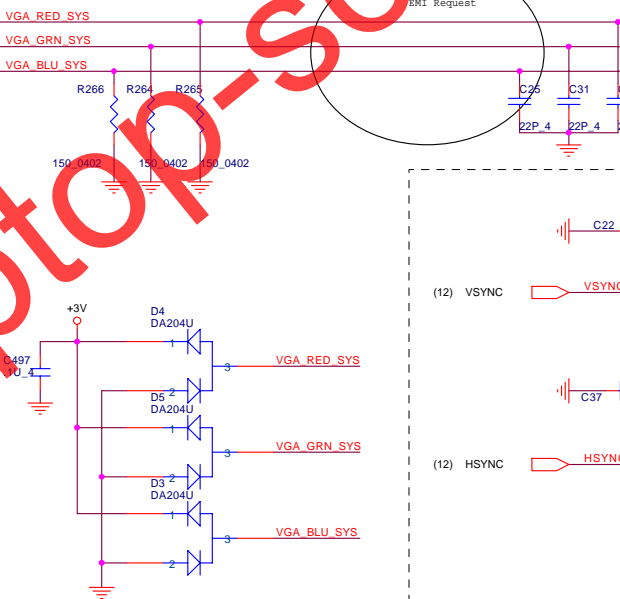
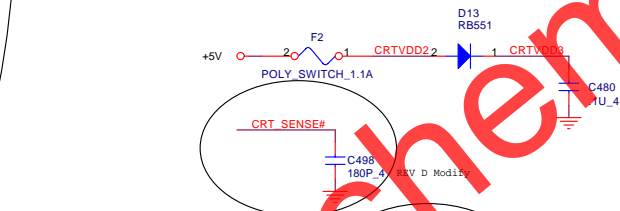
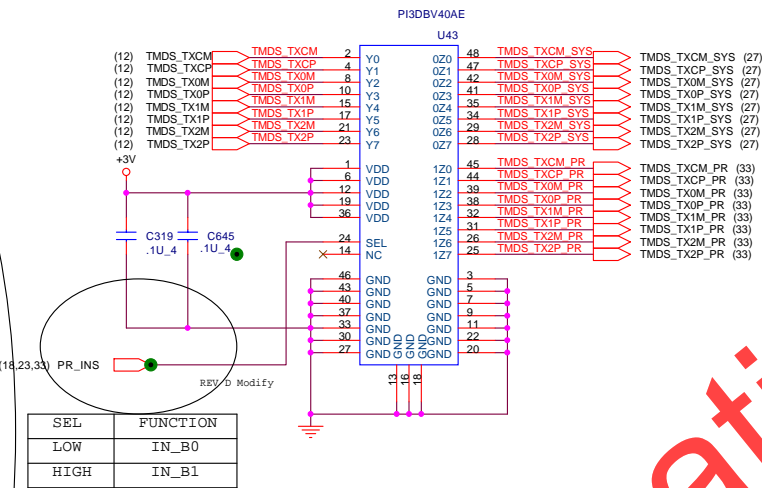
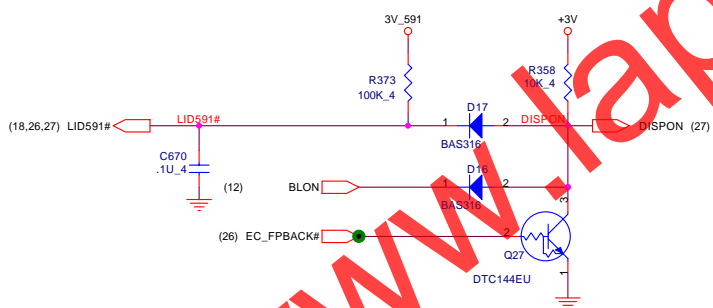
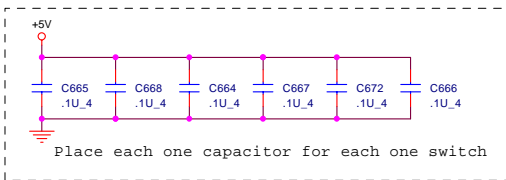
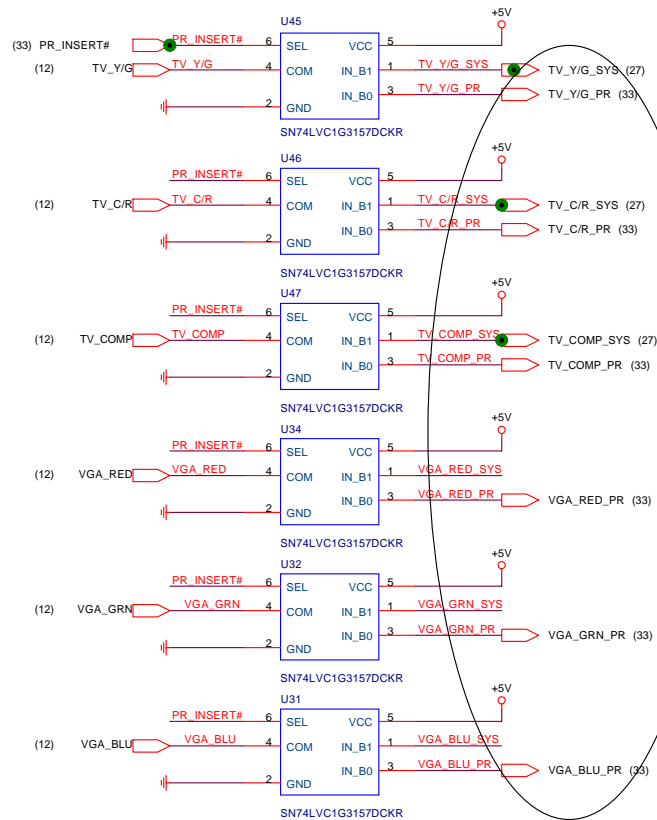
Place close to memory



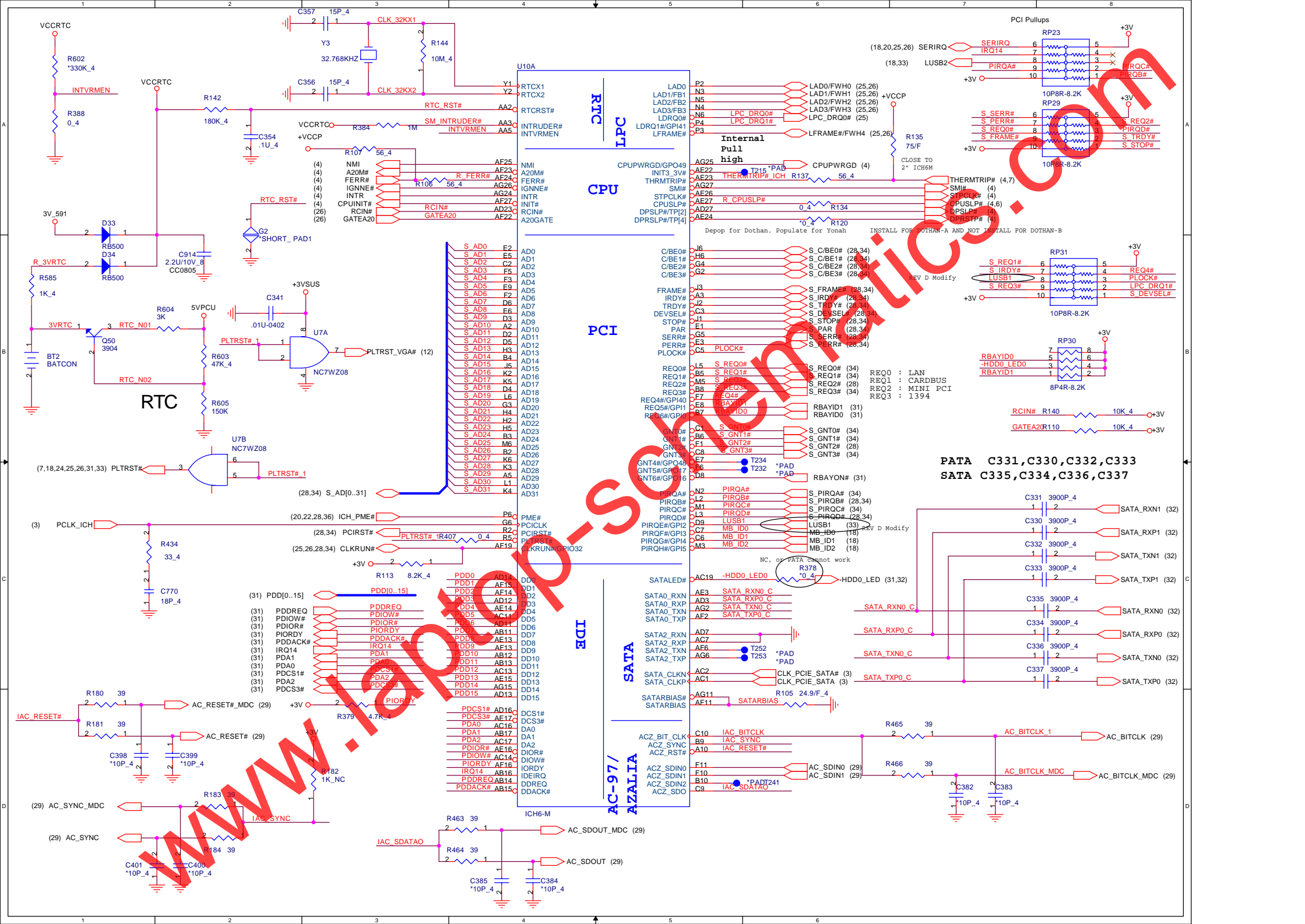
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

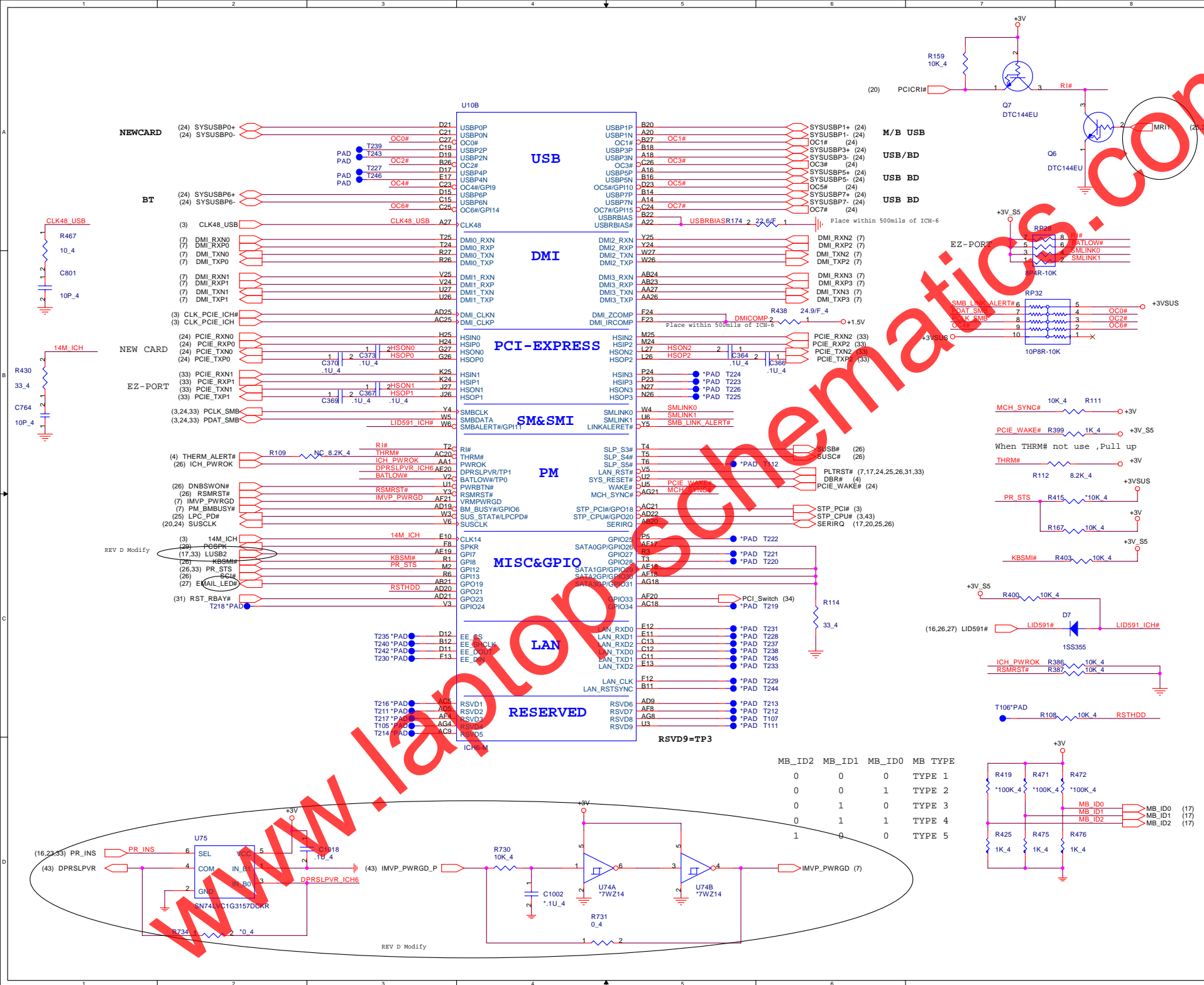


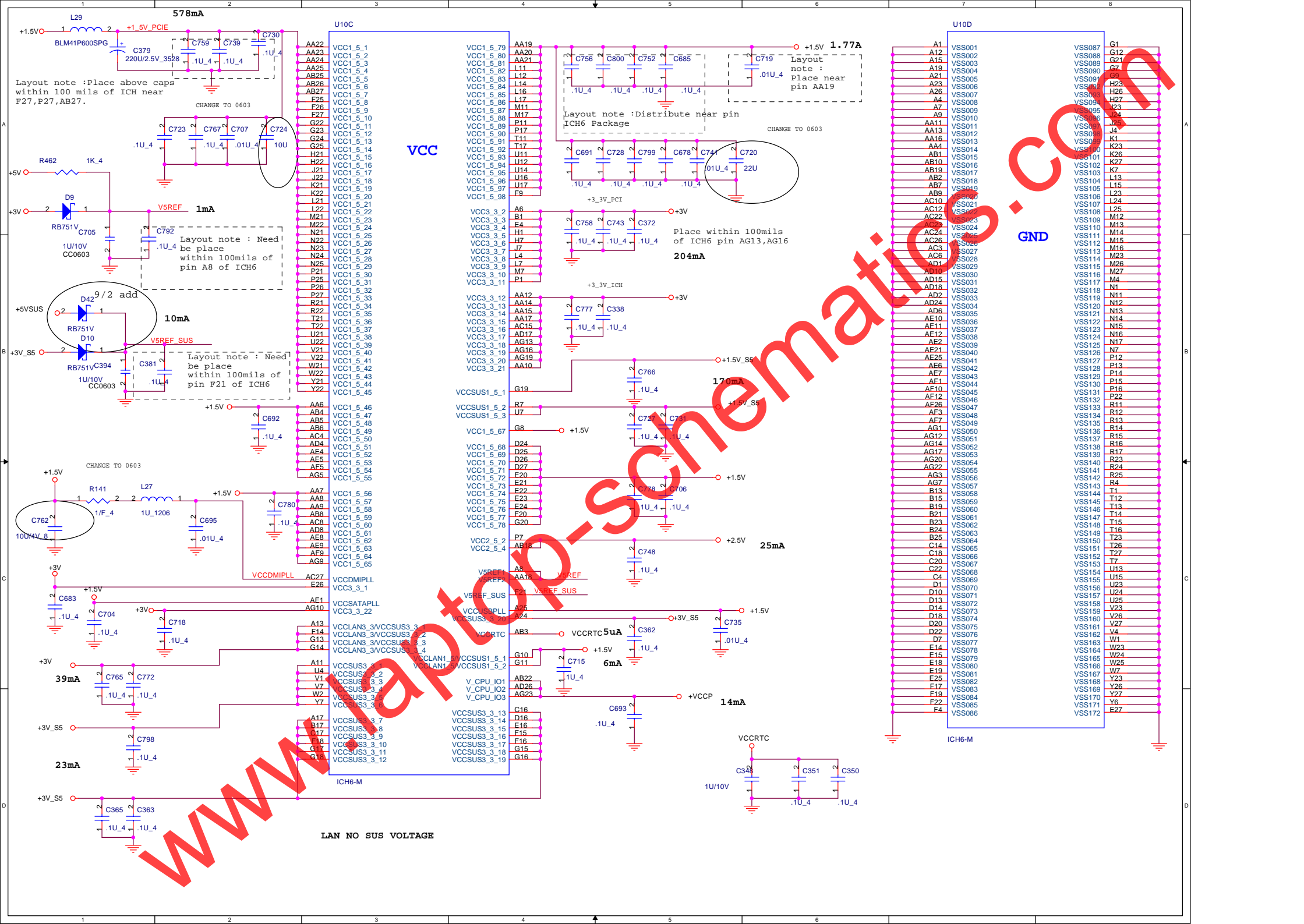
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

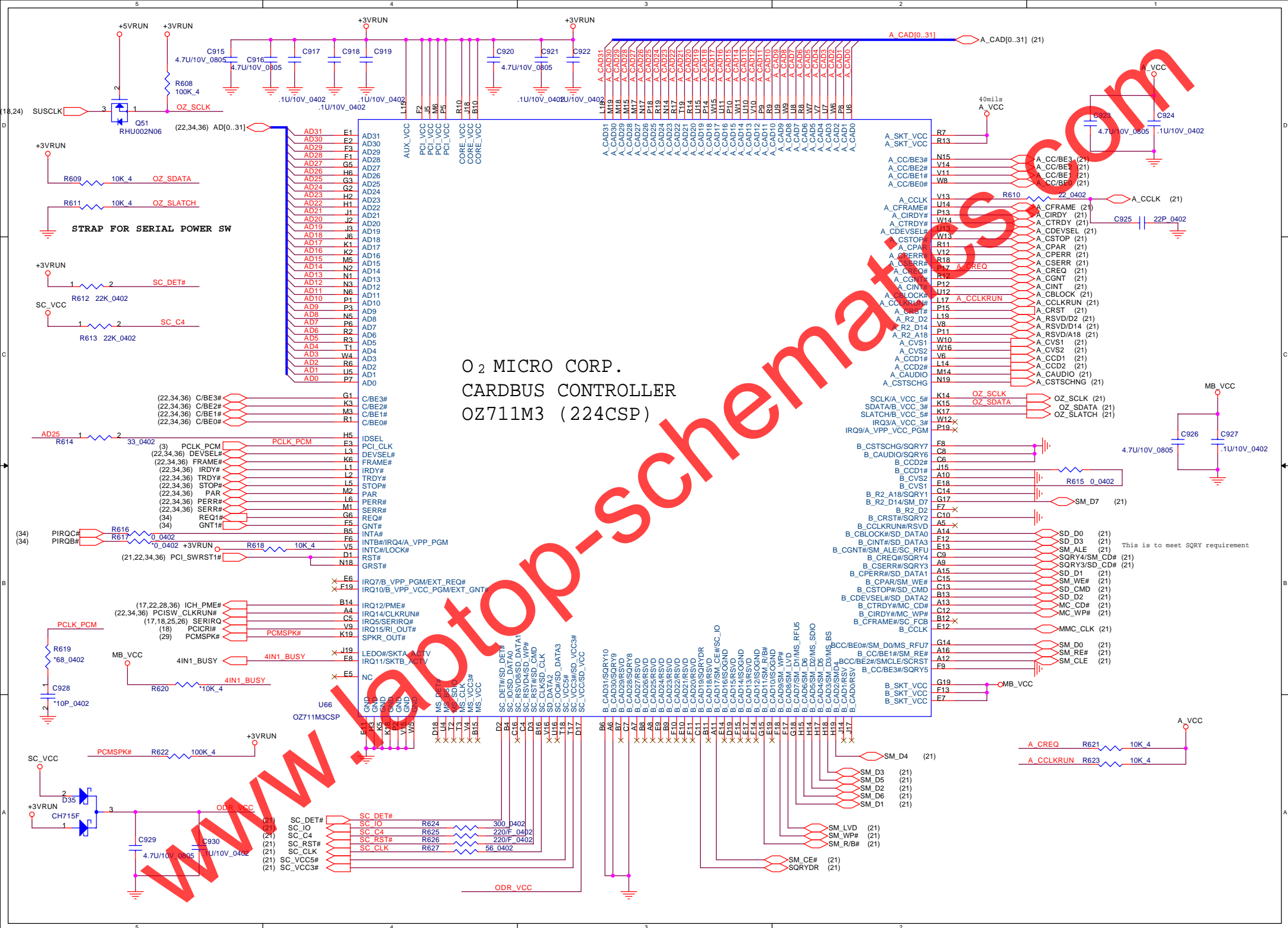


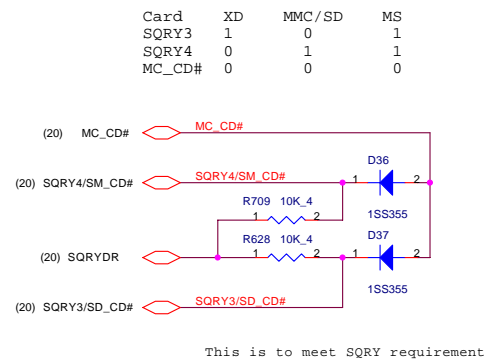
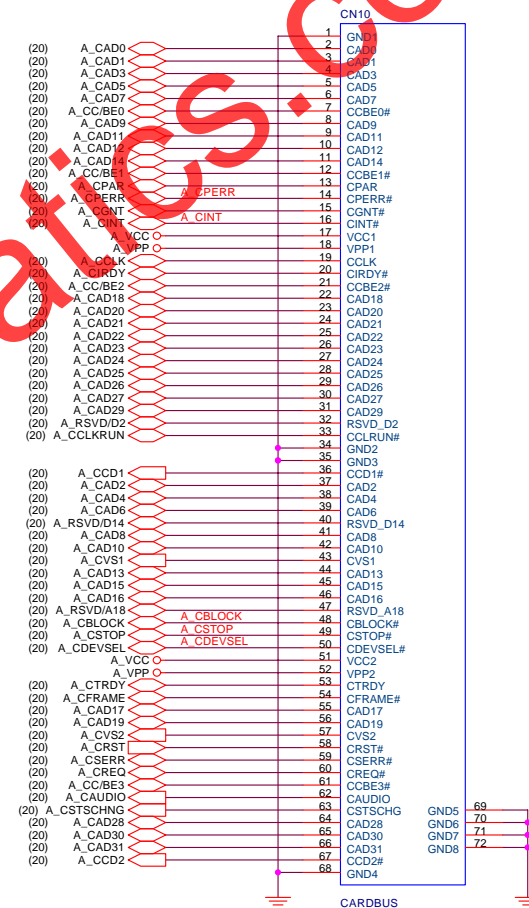
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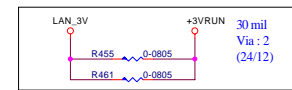






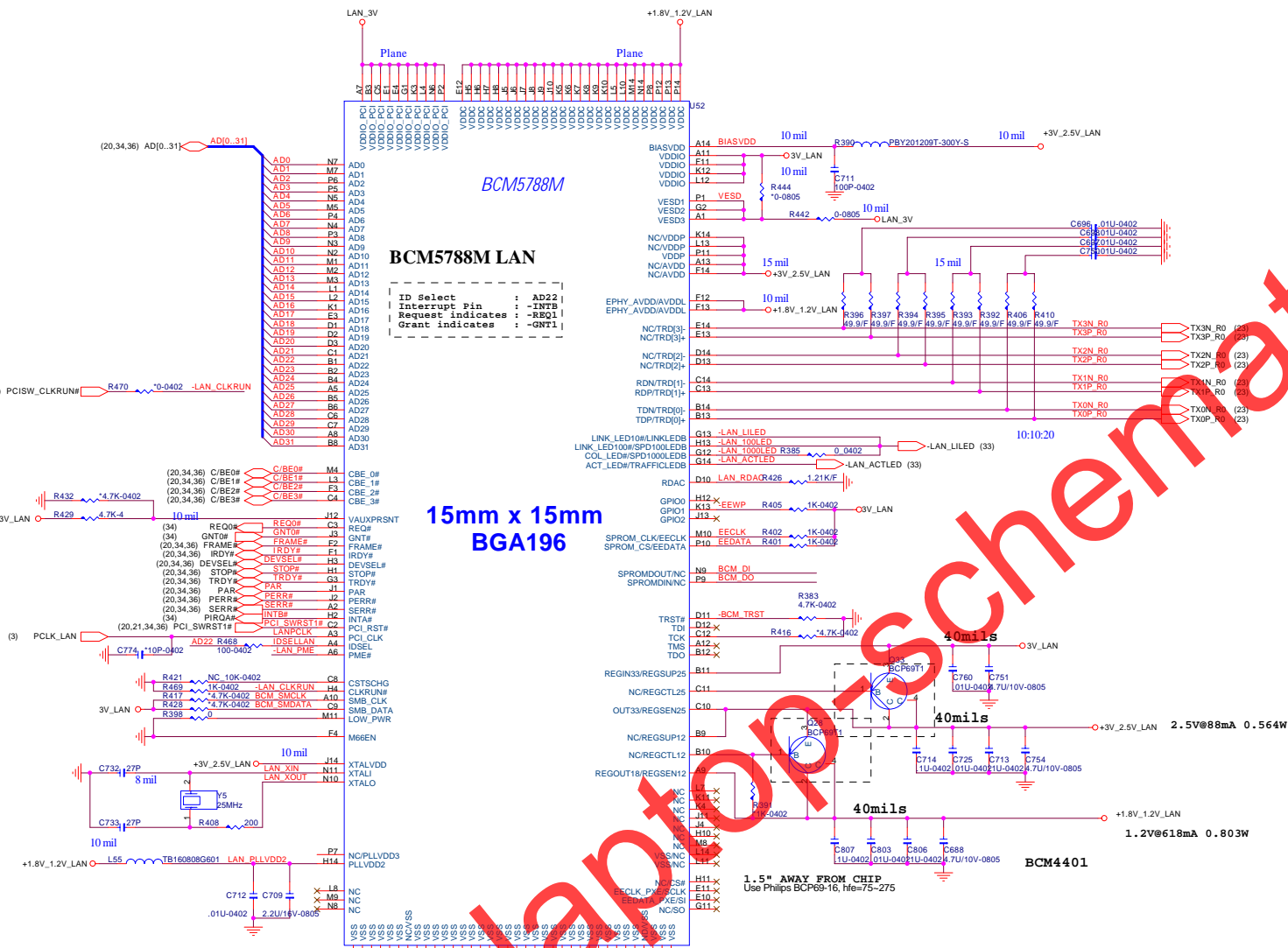


[illegible]



FOR 5788M(GIGA) USE

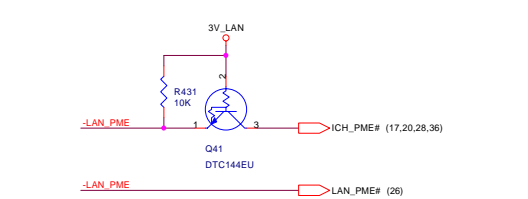
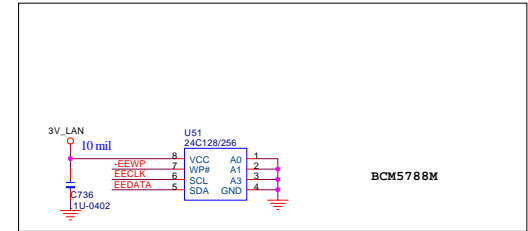
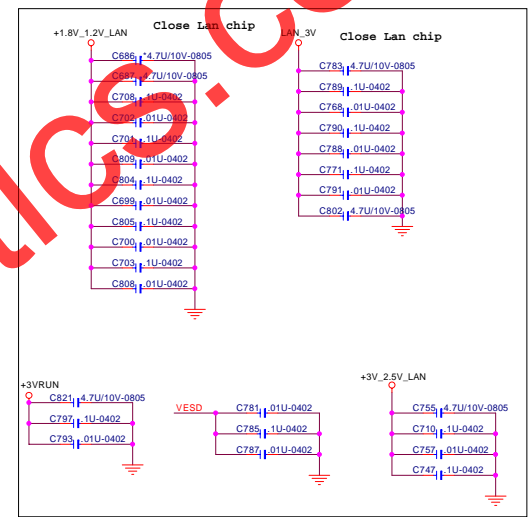
30 mil
Via: 2
(24/12)



BCM5788M LAN

ID Select : AD22
Interrupt Pin : INTB
Request indicates : -REQ1
Grant indicates : -GNT1

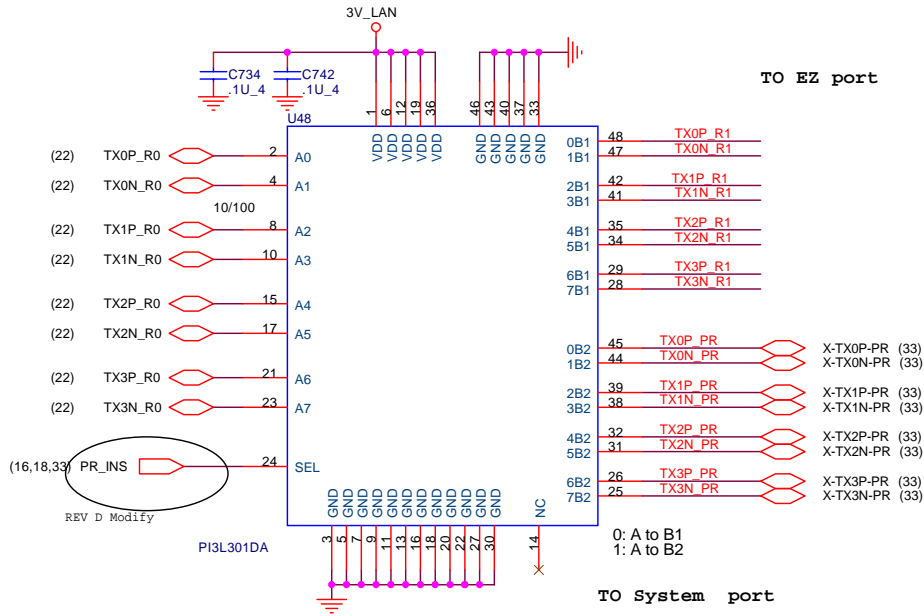
15mm x 15mm
BGA196



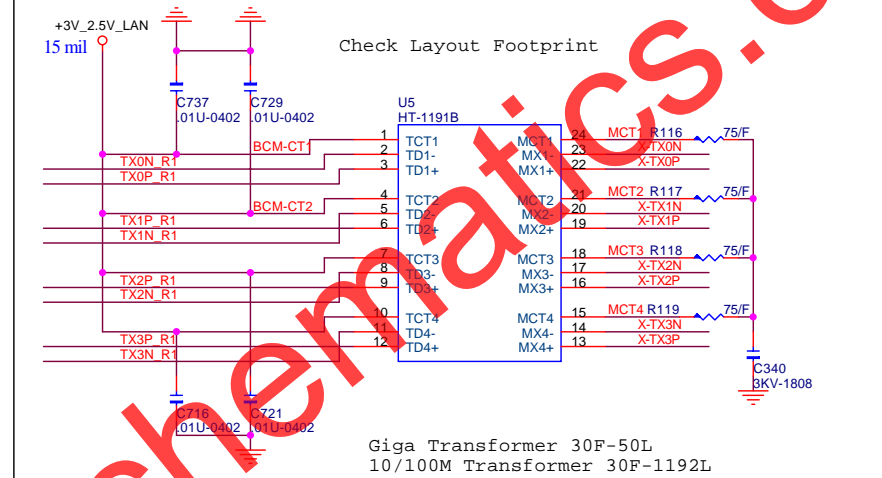
Voltage Rail	4401	5702	5705M
VDDIO_PCI	3V_S5	+3V	+3V
+3V_2.5V_LAN	3.3V	2.5V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V	1.2V

DNS	BCM4401	BCM5788M
STU	Q16,Q17,U26 R327,R329 R331,R332,U55	U55,R331,R332 Q16,Q17,U26

Lan Switch

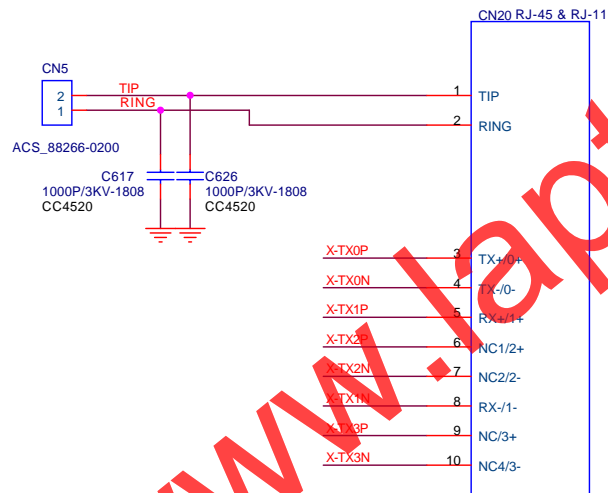


10/100/1000 M TRANSFORMER

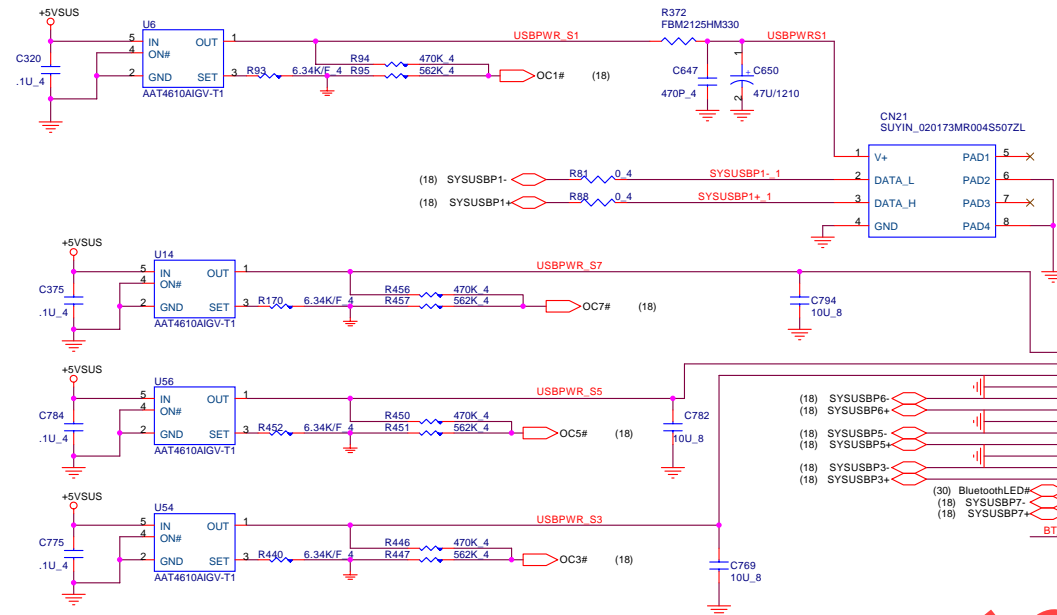


LAN and RJ11 Jack

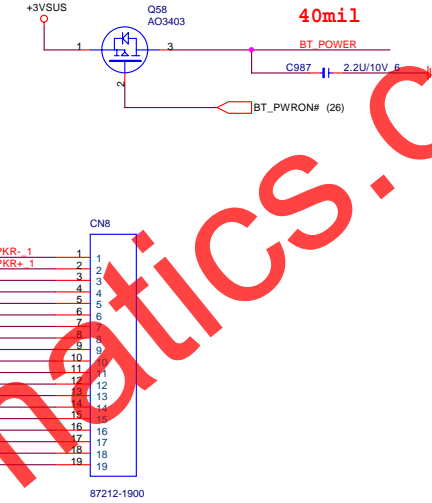
Check Layout Footprint



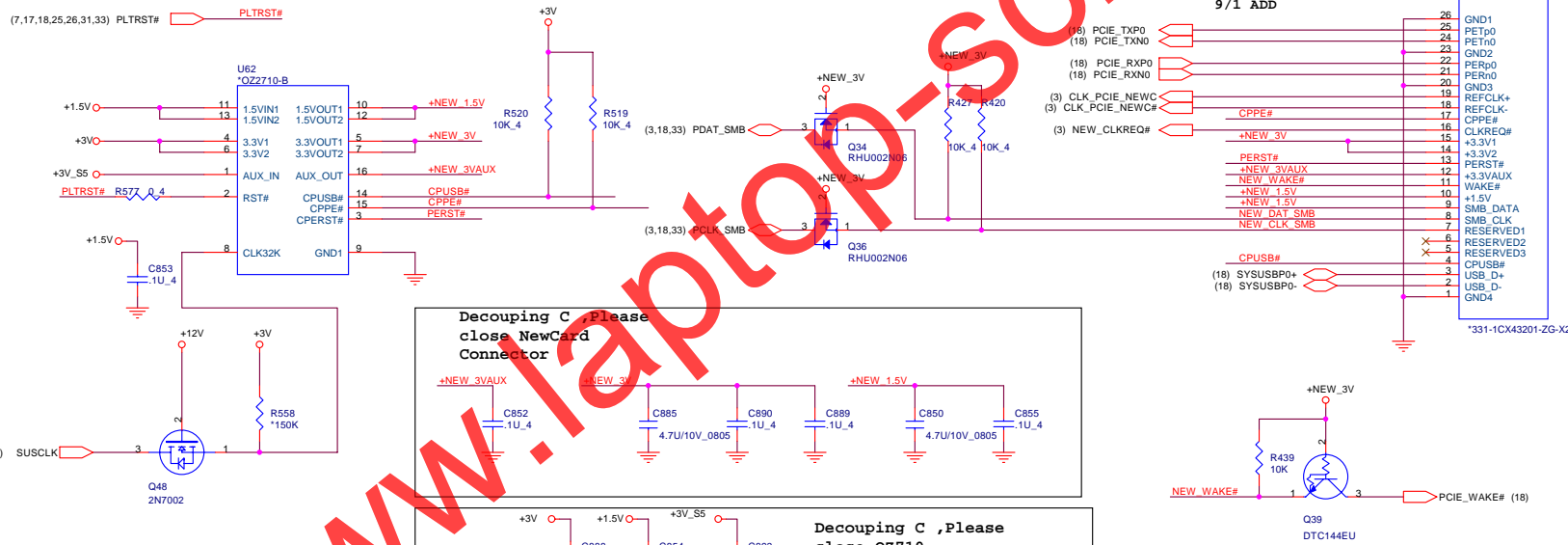
USB Connector and USB board

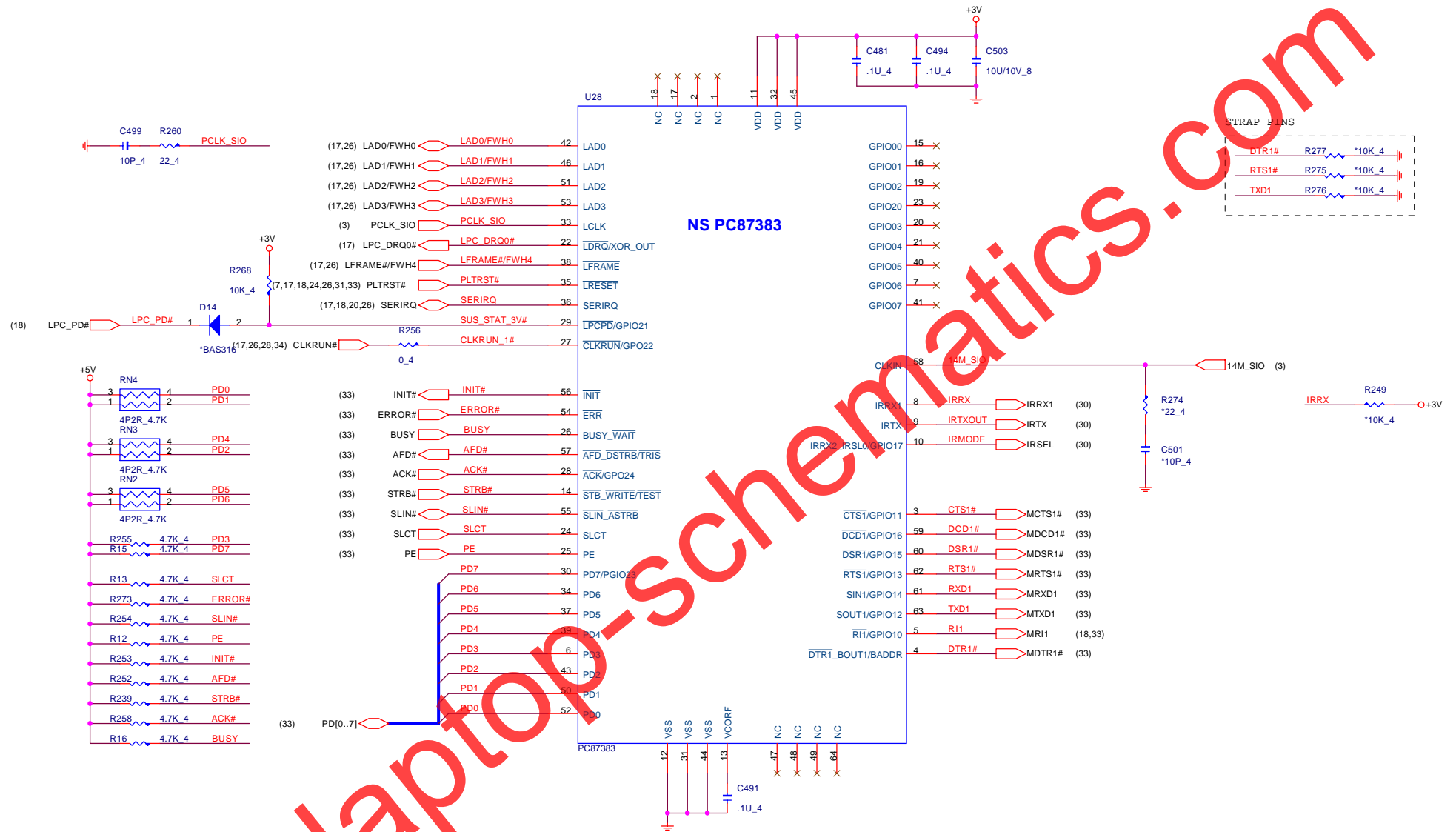


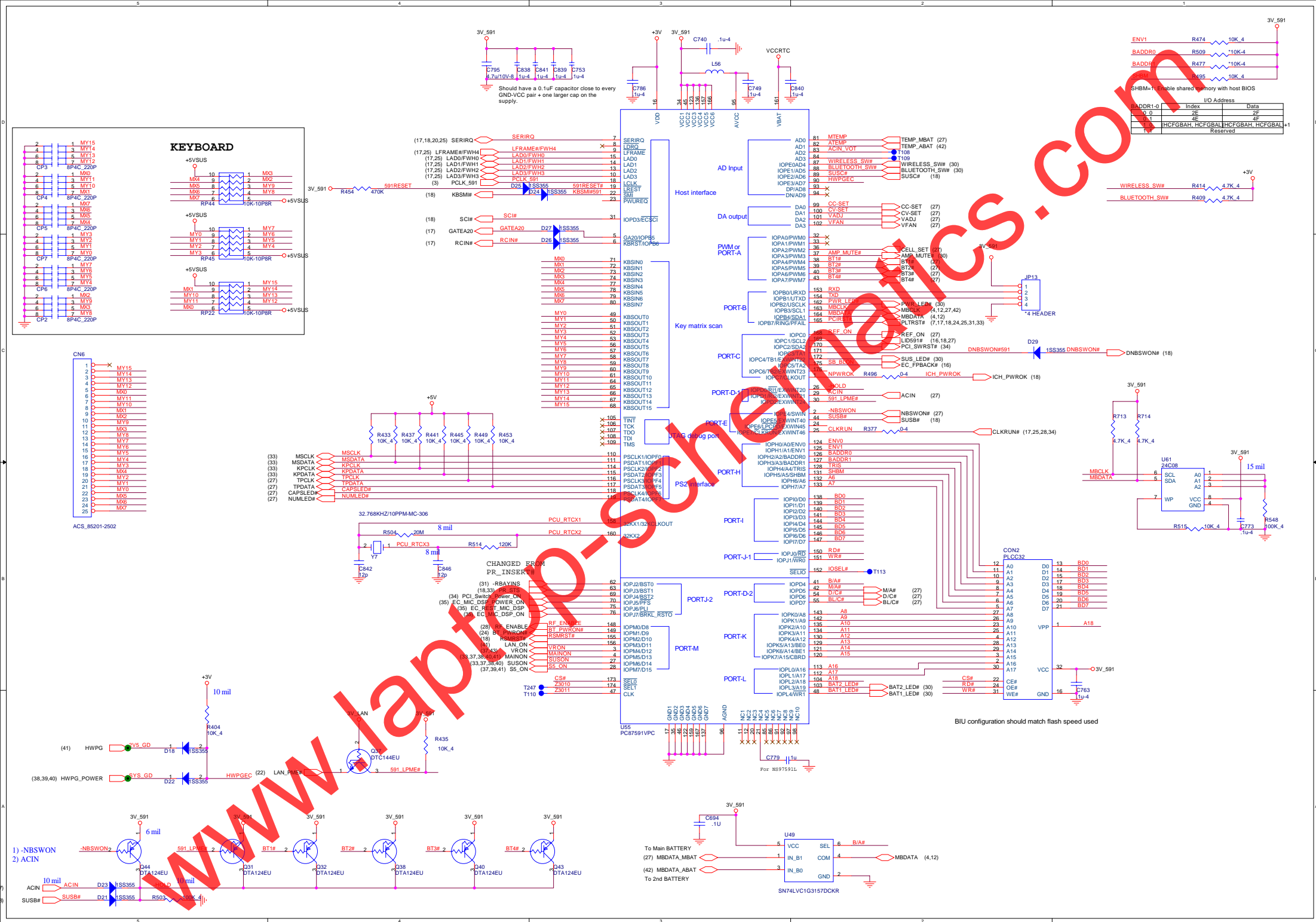
Bluetooth AND USB Connector



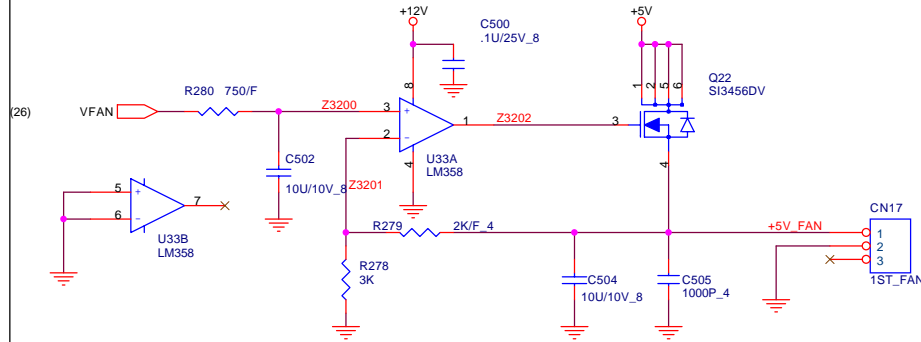
NewCard



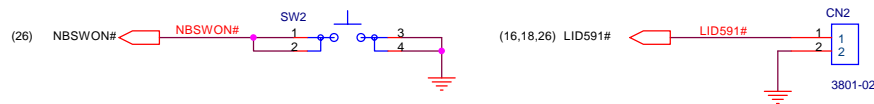




1st FAN OUT CONNECTOR

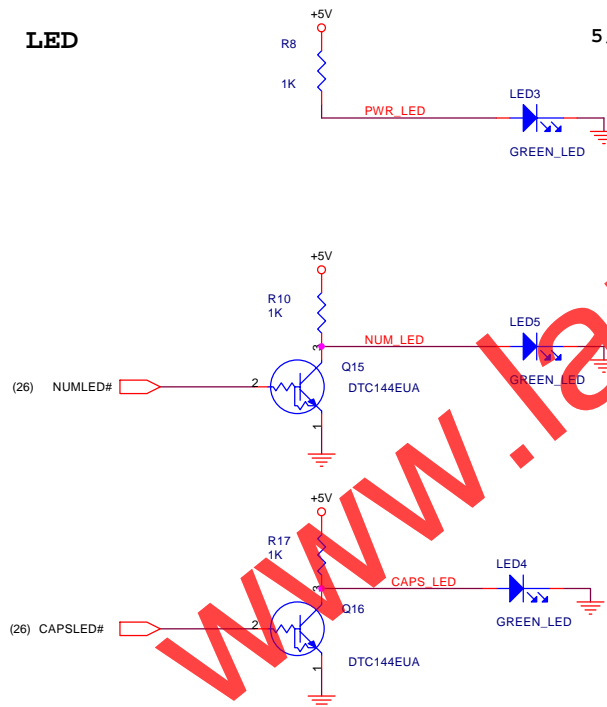


Power Switch

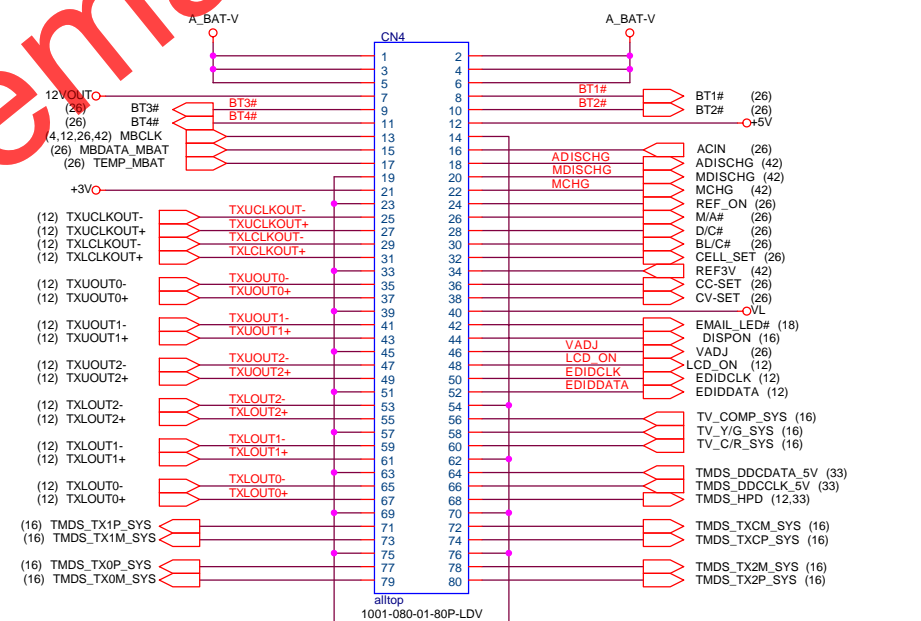
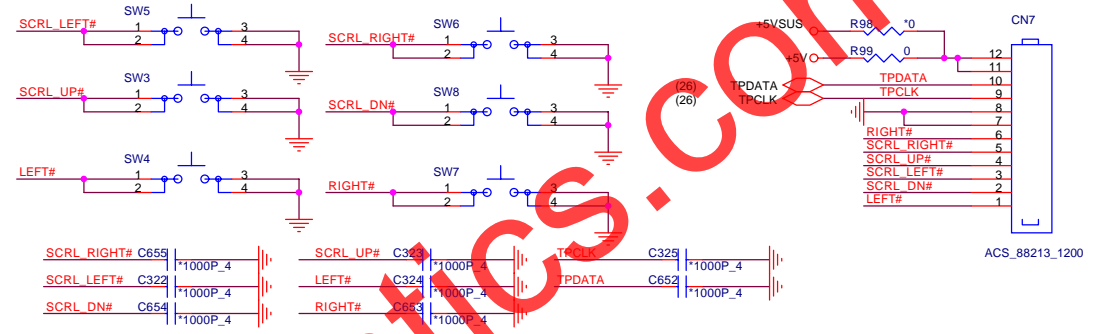


LED

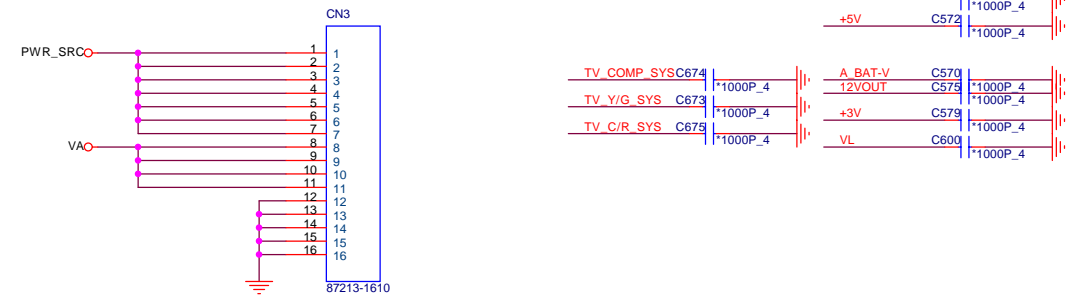
5/28 ADD

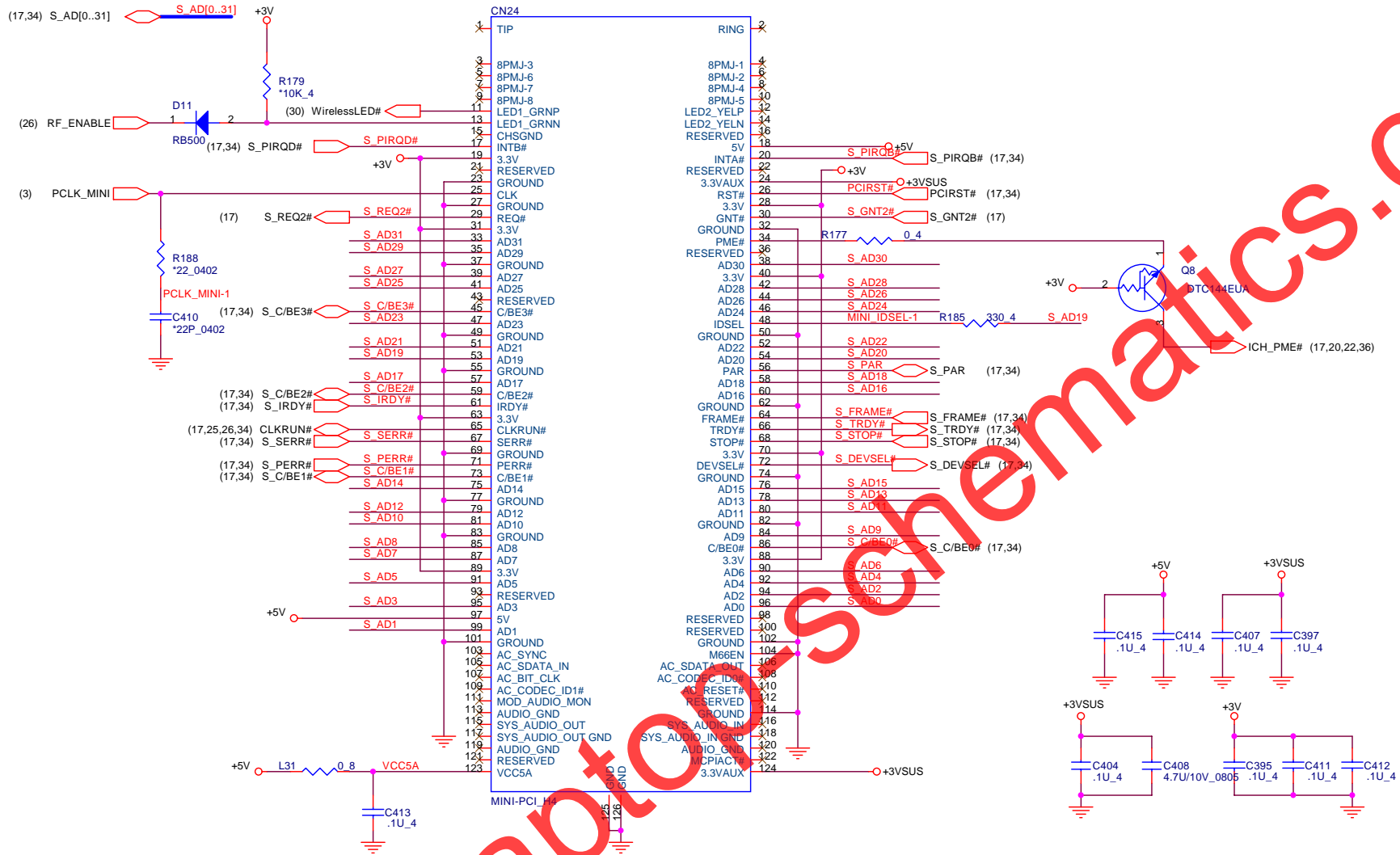


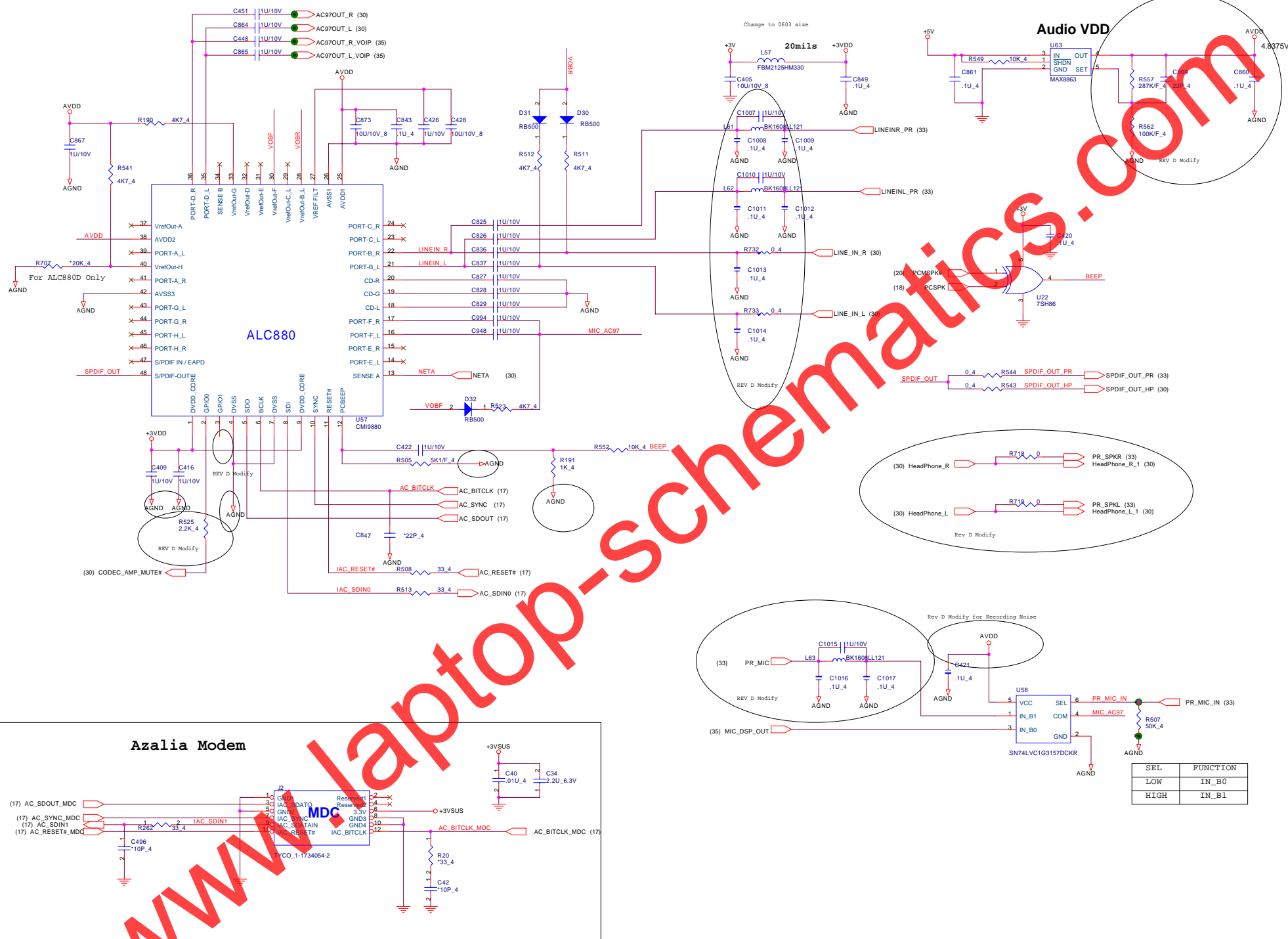
TouchPad Switch and T/P Module Connector



Power Connector







SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

Audio amplifier

SPKR MODE: 0.5DB, 9DB
HP MODE: 3, 0

INT. SPEAKER

Left_Speak(53398-0290)

Audio Board to Board Connector

REV B - Qualify

www.laptop-schematics.com

Audio amplifier

SPKR MODE HP MODE

0.5DB	3
9DB	0

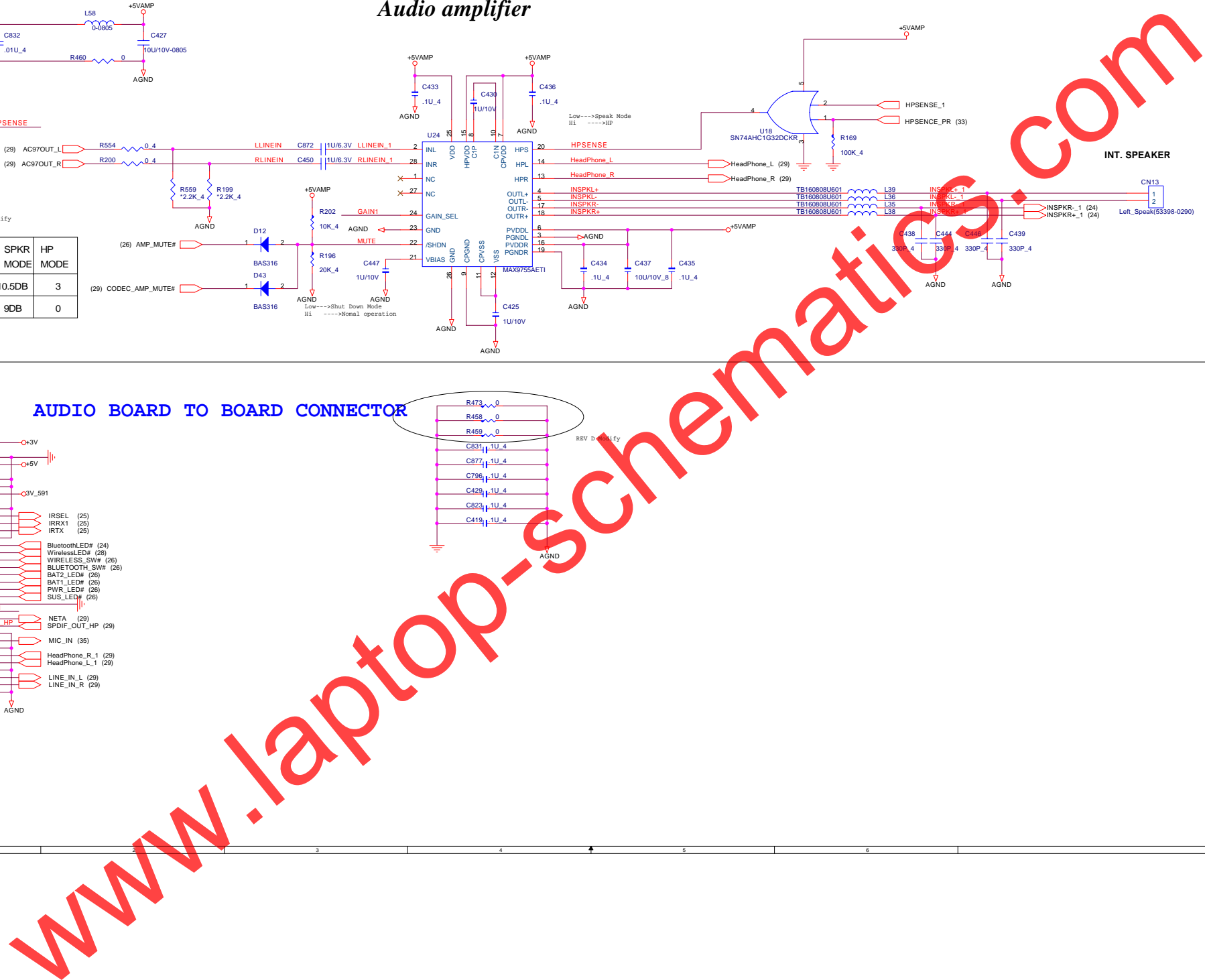
INT. SPEAKER

Left_Speak(53398-0290)

AUDIO BOARD TO BOARD CONNECTOR

IRSEL (25)	IRRX1 (25)	IRTX (25)
BluetoothLED# (24)	WirelessLED# (28)	WIRELESS_SW# (26)
BAT2_LED# (26)	BAT1_LED# (26)	PWR_LED# (26)
SUS_LED# (26)	NETA (29)	SPDIF_OUT_HP (29)
MIC_IN (35)	HeadPhone_R_1 (29)	HeadPhone_L_1 (29)
LINE_IN_L (29)	LINE_IN_R (29)	

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SWAP BAY POWER CONTROL & RESET

(17) RBAYON#

(18) RST_RBAY#

(7,17,18,24,25,26,33) PLTRST#

[illegible]

Multi-Bay Connector

The diagram illustrates the electrical connections for a Multi-Bay Connector. It includes a pinout table on the left, a detailed wiring schematic in the center, and a BAY ID STATUS table on the right.

Pinout Table:

Signal	Pin
PDD[0..15]	(17)
PDDREQ	(17)
PDIOW#	(17)
PDIOR#	(17)
PORDY	(17)
PDDACK#	(17)
IRQ14	(17)
PDA1	(17)
PDA0	(17)
PDCS1#	(17)
PDA2	(17)
PDCS3#	(17)

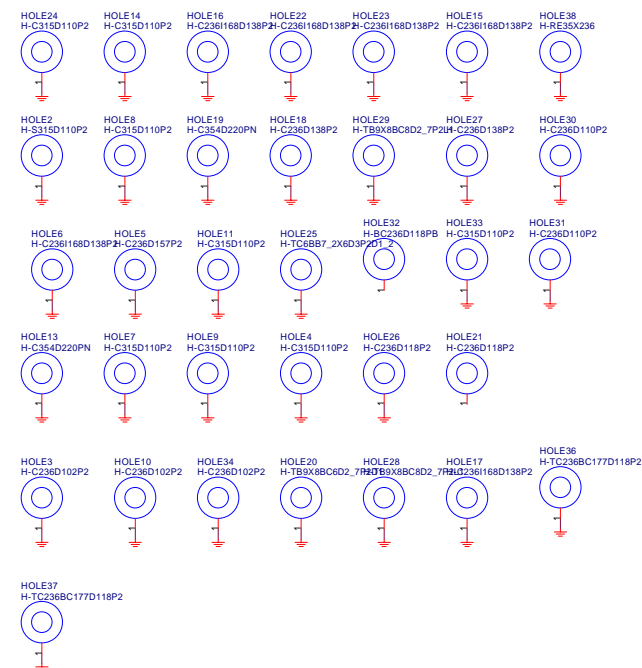
Wiring Schematic:

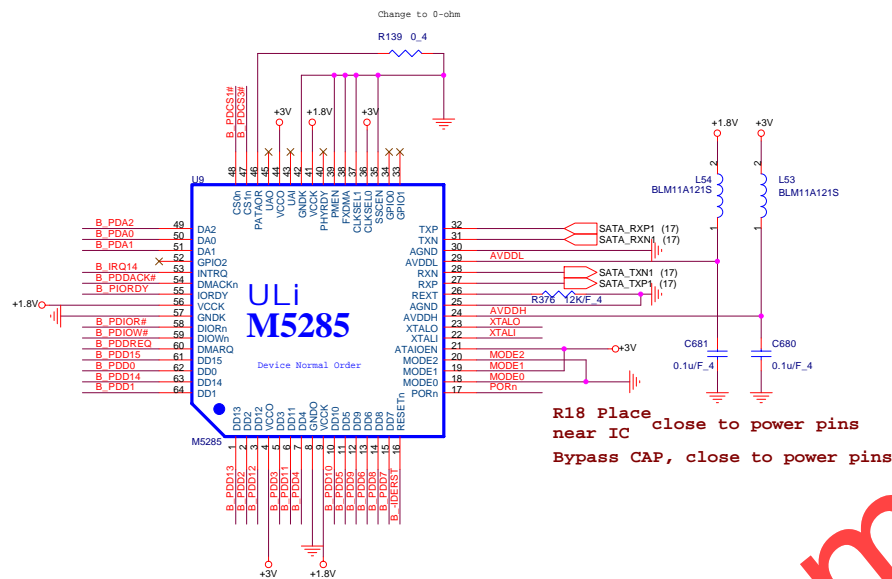
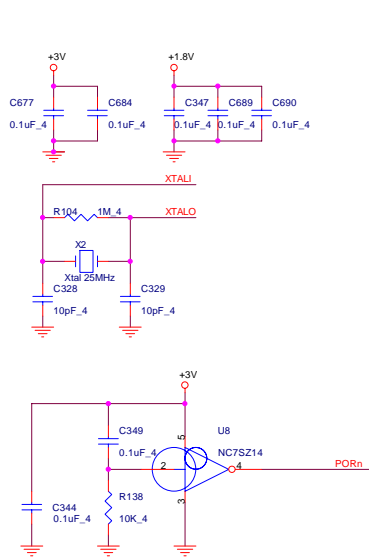
- Power and Ground:** 3V_501 is connected to pin 1 through R27 (10K_4). Pin 2 is connected to ground through R26 (1K). Pin 3 is connected to ground through C93 (.1U).
- Signal Connections:**
 - PDD[0..15] is connected to pins 1-16.
 - PDDREQ is connected to pin 17.
 - PDIOW# is connected to pin 18.
 - PDIOR# is connected to pin 19.
 - PORDY is connected to pin 20.
 - PDDACK# is connected to pin 21.
 - IRQ14 is connected to pin 22.
 - PDA1 is connected to pin 23.
 - PDA0 is connected to pin 24.
 - PDCS1# is connected to pin 25.
 - PDA2 is connected to pin 26.
 - PDCS3# is connected to pin 27.
- Other Connections:**
 - Pin 28 is connected to T6 PAD.
 - Pin 29 is connected to CN19.
 - Pin 30 is connected to *PAD T7.
 - Pin 31 is connected to *PAD T8.
 - Pin 32 is connected to RST RBAY0.
 - Pin 33 is connected to PDB7.
 - Pin 34 is connected to PDB6.
 - Pin 35 is connected to PDB5.
 - Pin 36 is connected to PDB4.
 - Pin 37 is connected to PDB3.
 - Pin 38 is connected to PDB2.
 - Pin 39 is connected to PDB1.
 - Pin 40 is connected to PDB0.
 - Pin 41 is connected to PDI07.
 - Pin 42 is connected to PDI06.
 - Pin 43 is connected to PDI05.
 - Pin 44 is connected to PDI04.
 - Pin 45 is connected to PDI03.
 - Pin 46 is connected to PDI02.
 - Pin 47 is connected to PDI01.
 - Pin 48 is connected to PDI00.
 - Pin 49 is connected to PDIOR#.
 - Pin 50 is connected to PDDACK#.
 - Pin 51 is connected to PDA1.
 - Pin 52 is connected to PDA0.
 - Pin 53 is connected to PDCS3#.
 - Pin 54 is connected to PDA2.
 - Pin 55 is connected to PDCS1#.
 - Pin 56 is connected to PDCS3#.
 - Pin 57 is connected to RBAYID0 (17).
 - Pin 58 is connected to RBAYID1 (17).
 - Pin 59 is connected to RBAYVCC.
 - Pin 60 is connected to RCSEL.
 - Pin 61 is connected to RCSEL MASTER.
 - Pin 62 is connected to ADD.
 - Pin 63 is connected to R34.
 - Pin 64 is connected to R283 (1).
 - Pin 65 is connected to R283 (2).
 - Pin 66 is connected to R283 (4).
 - Pin 67 is connected to R283 (7).
 - Pin 68 is connected to R283 (10).
 - Pin 69 is connected to R283 (13).
 - Pin 70 is connected to R283 (16).
 - Pin 71 is connected to R283 (19).
 - Pin 72 is connected to R283 (22).
 - Pin 73 is connected to R283 (25).
 - Pin 74 is connected to R283 (28).
 - Pin 75 is connected to R283 (31).
 - Pin 76 is connected to R283 (34).
 - Pin 77 is connected to R283 (37).
 - Pin 78 is connected to R283 (40).
 - Pin 79 is connected to R283 (43).
 - Pin 80 is connected to R283 (46).
 - Pin 81 is connected to R283 (49).
 - Pin 82 is connected to R283 (52).
 - Pin 83 is connected to R283 (55).
 - Pin 84 is connected to R283 (58).
 - Pin 85 is connected to R283 (61).
 - Pin 86 is connected to R283 (64).
 - Pin 87 is connected to R283 (67).
 - Pin 88 is connected to R283 (70).
 - Pin 89 is connected to R283 (73).
 - Pin 90 is connected to R283 (76).
 - Pin 91 is connected to R283 (79).
 - Pin 92 is connected to R283 (82).
 - Pin 93 is connected to R283 (85).
 - Pin 94 is connected to R283 (88).
 - Pin 95 is connected to R283 (91).
 - Pin 96 is connected to R283 (94).
 - Pin 97 is connected to R283 (97).
 - Pin 98 is connected to R283 (100).
 - Pin 99 is connected to R283 (103).
 - Pin 100 is connected to R283 (106).

BAY ID STATUS Table:

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD

BAY ID STATUS		
RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD



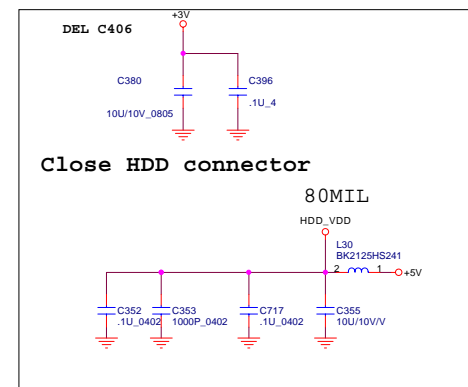
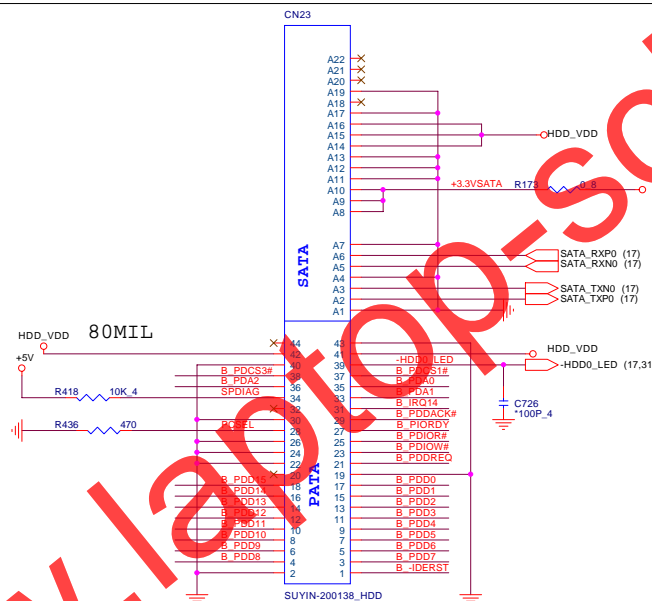


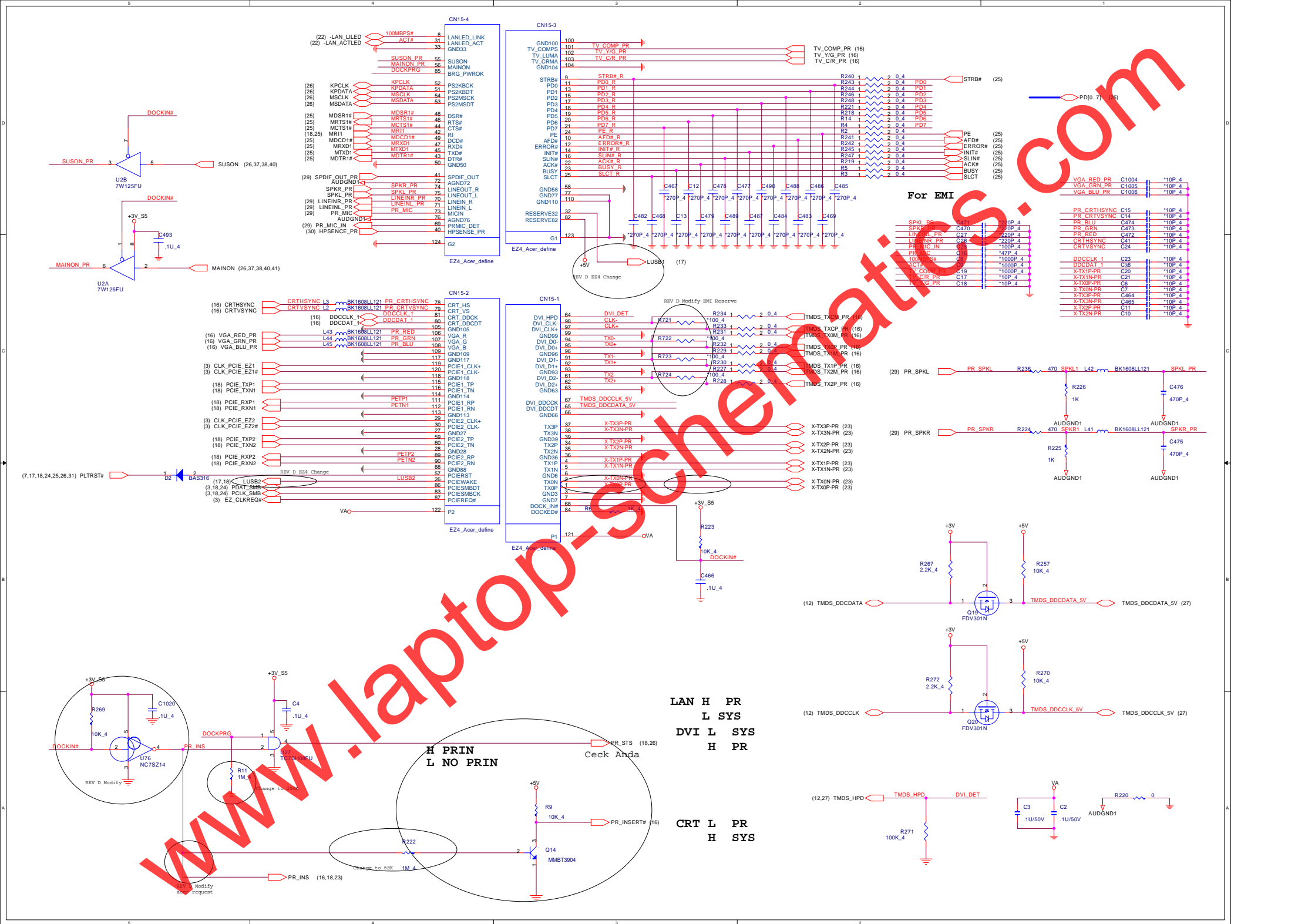
Operation Mode

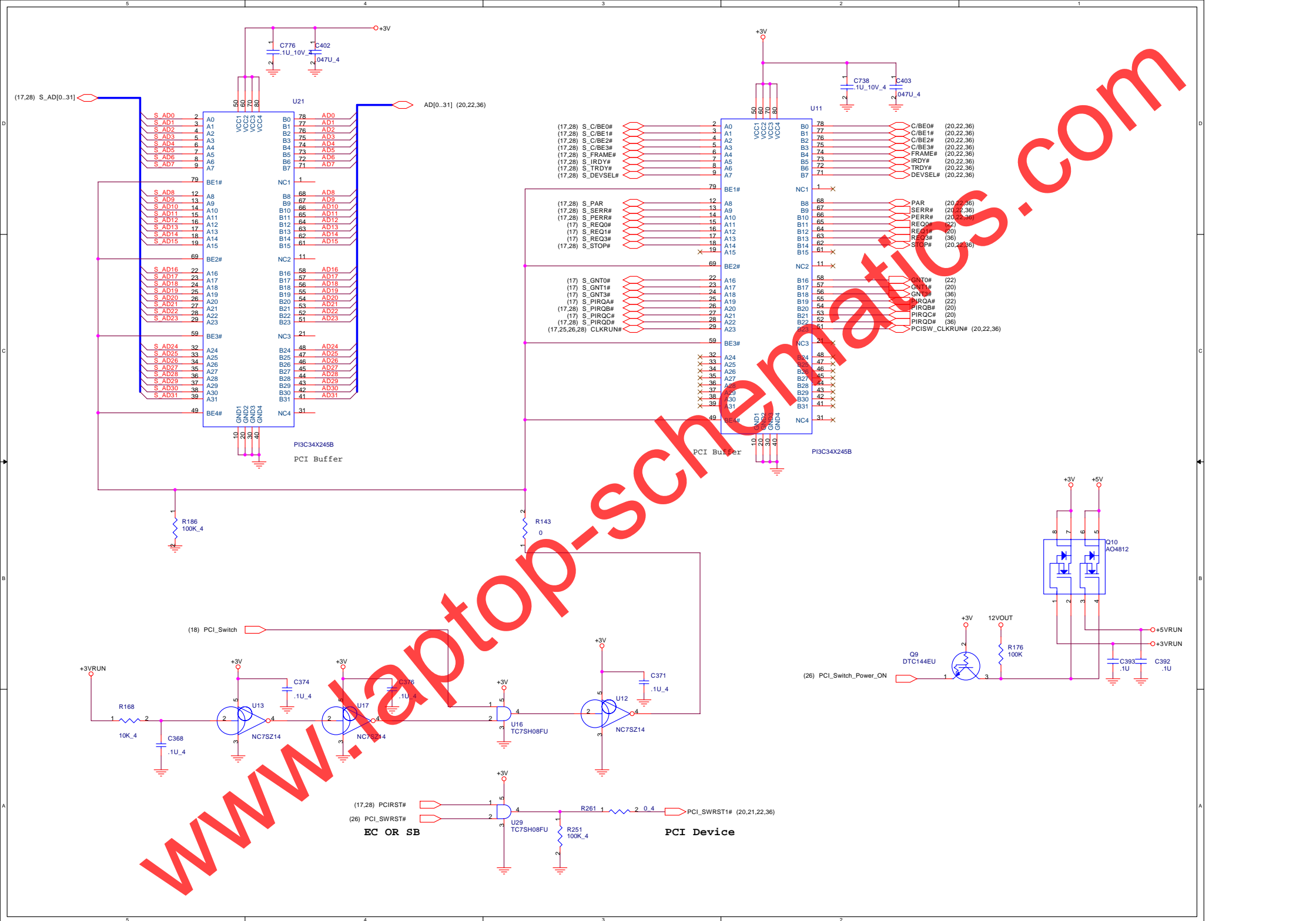
MODE[2..0]	Device mode
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	Device mode 150MB/S
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVE

Reference clock select

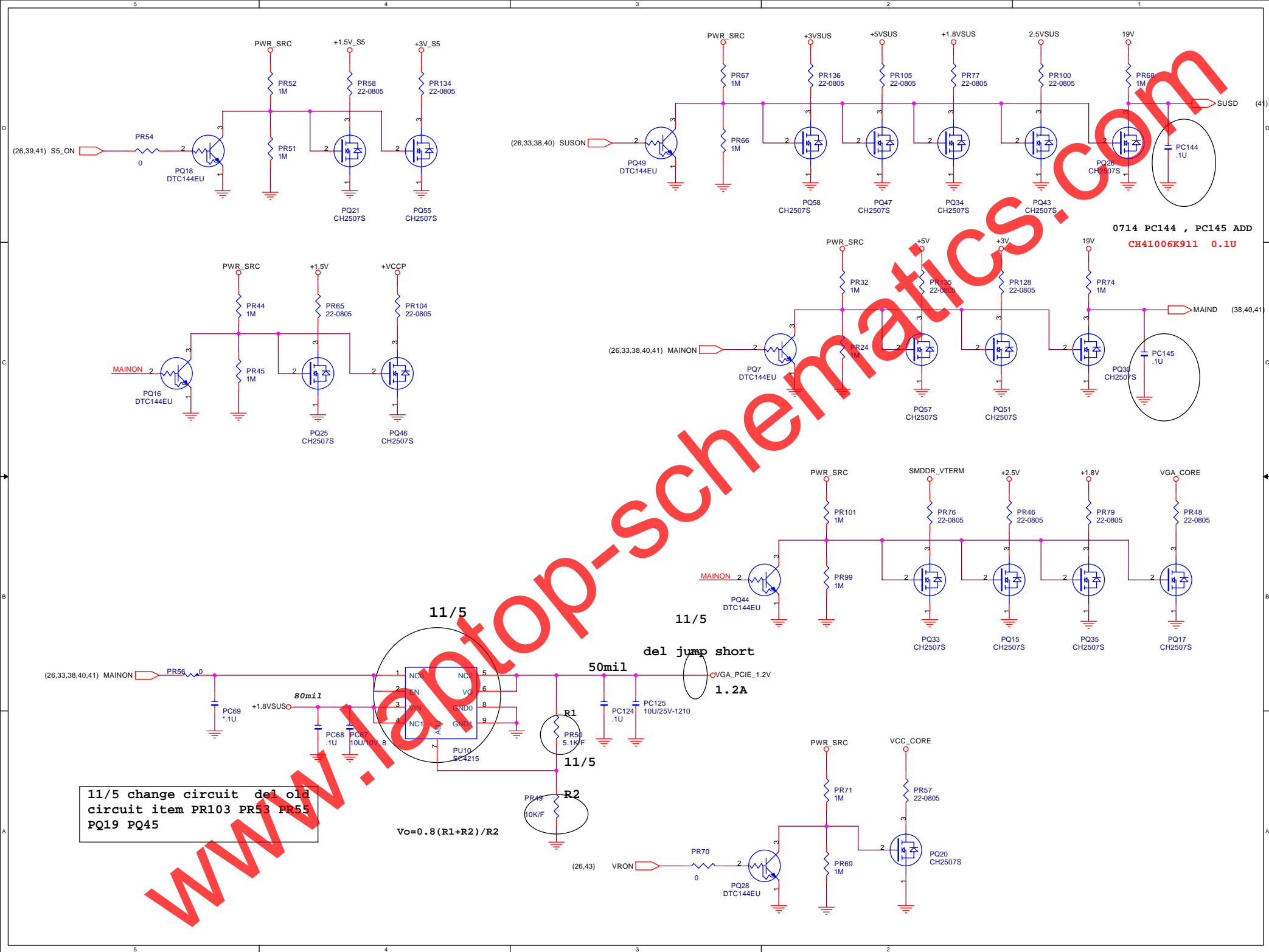
CLKSEL[1..0]	External clock
0 0	20 MHz
0 1	25 MHz

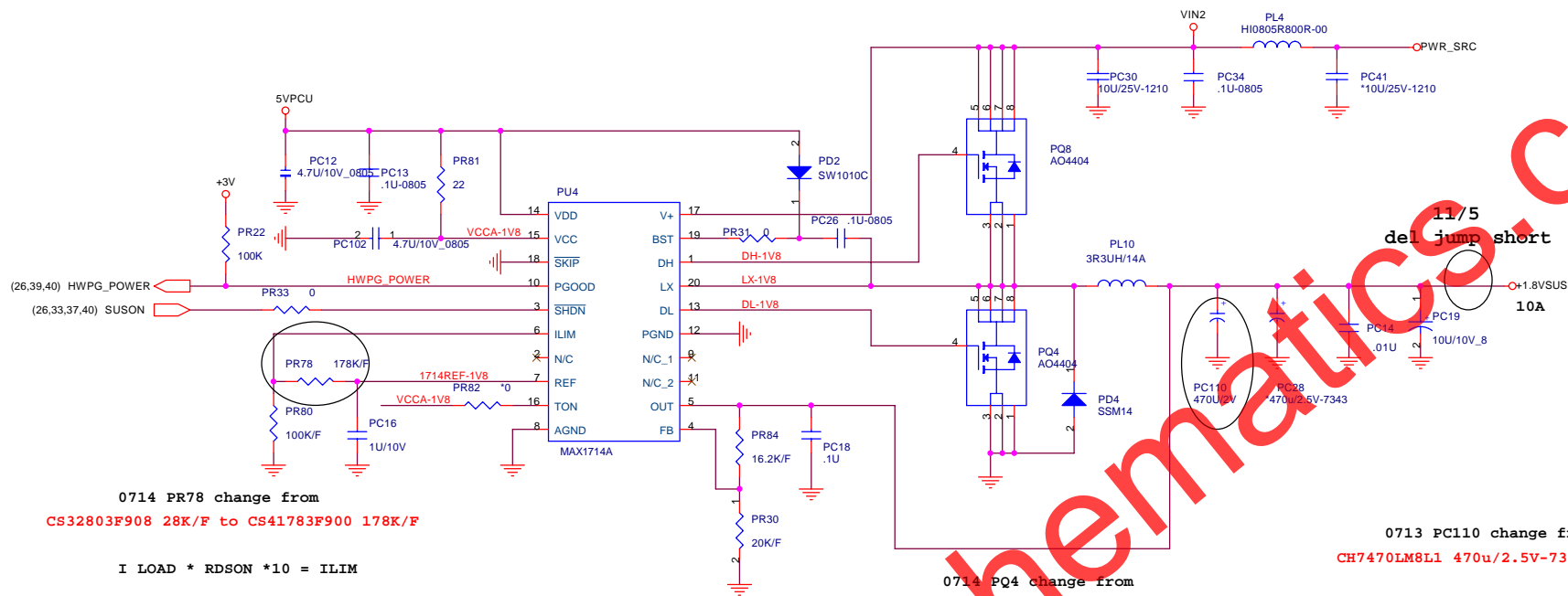








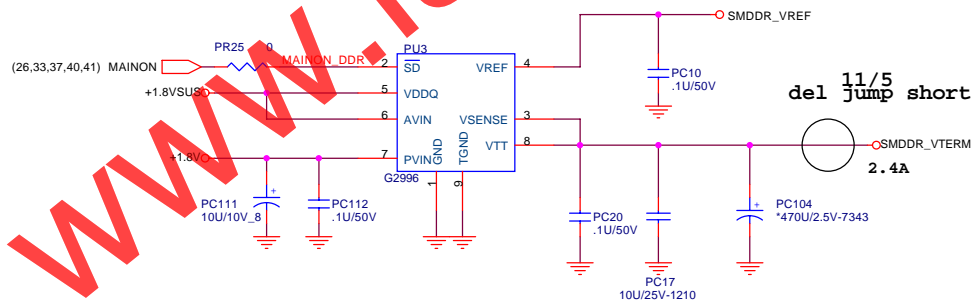
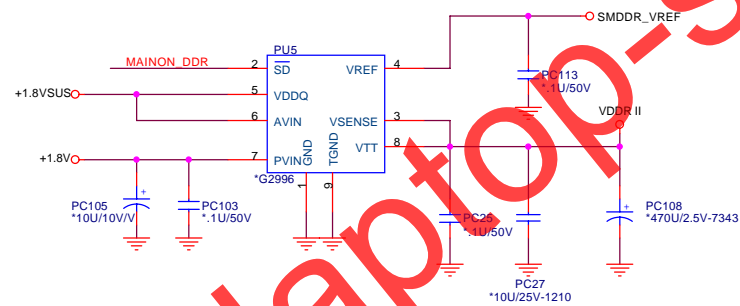




$I_{LOAD} * R_{DS(on)} * 10 = I_{LIM}$

FDD6688 $R_{DS(on)} 4.5V = 0.006 \text{ ohm}$

$12 * 0.006 * 10 = 0.72V (I_{LIM})$



0714 PR37 change from
CS21823F902 1.82K/F to CS27683F909 7.68K/F

0714 PL13 change from
CV-15A0MZ05 1R5 to CV-33E0MZ01 3R3

0714 PQ11 change from
BAM44040012 AO4404 to BAM60300Z11 FDD6030L

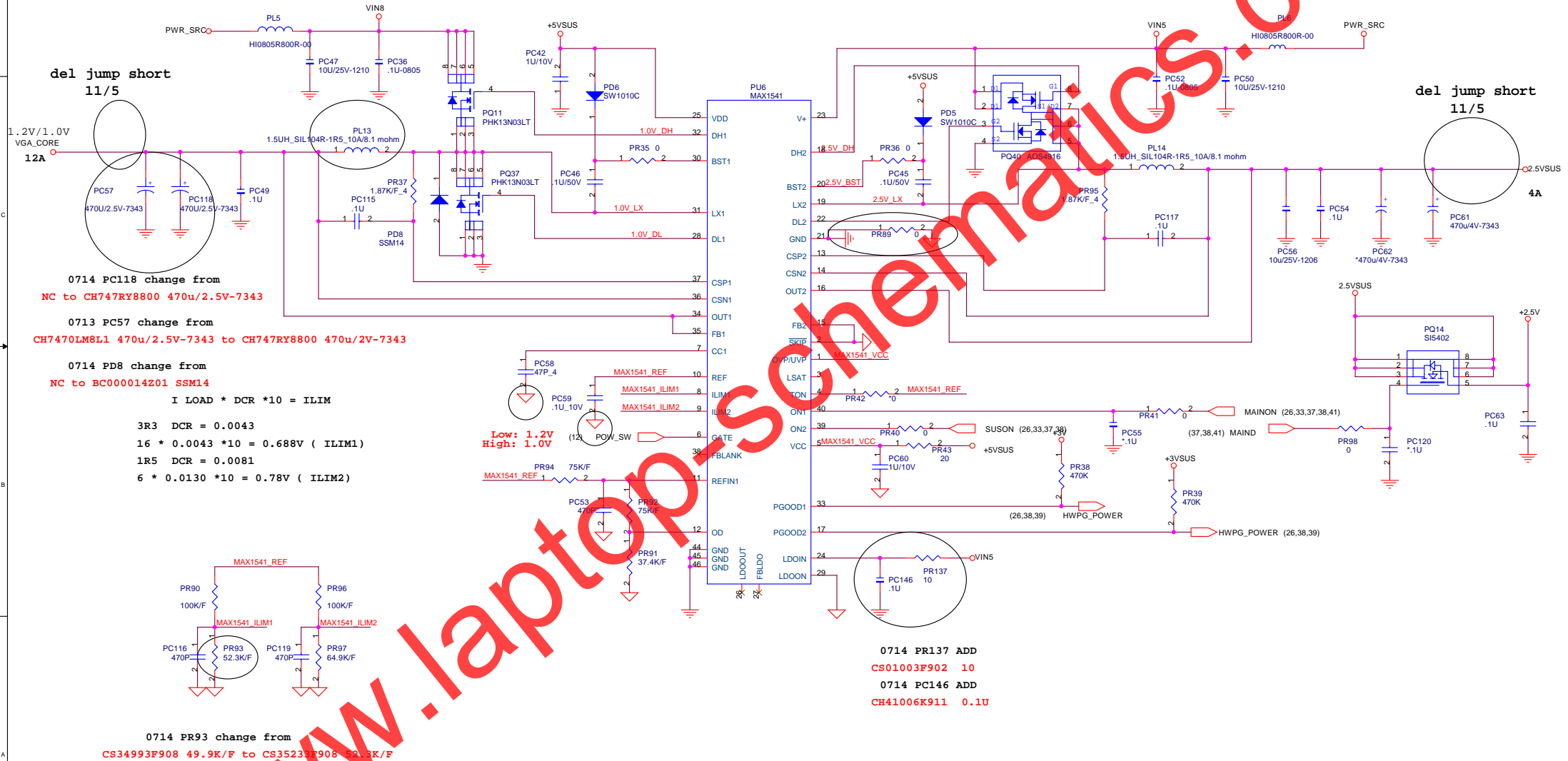
0714 PQ37 change from
BAM47040005 AO4704 to BAM6680Z01 FDD6688

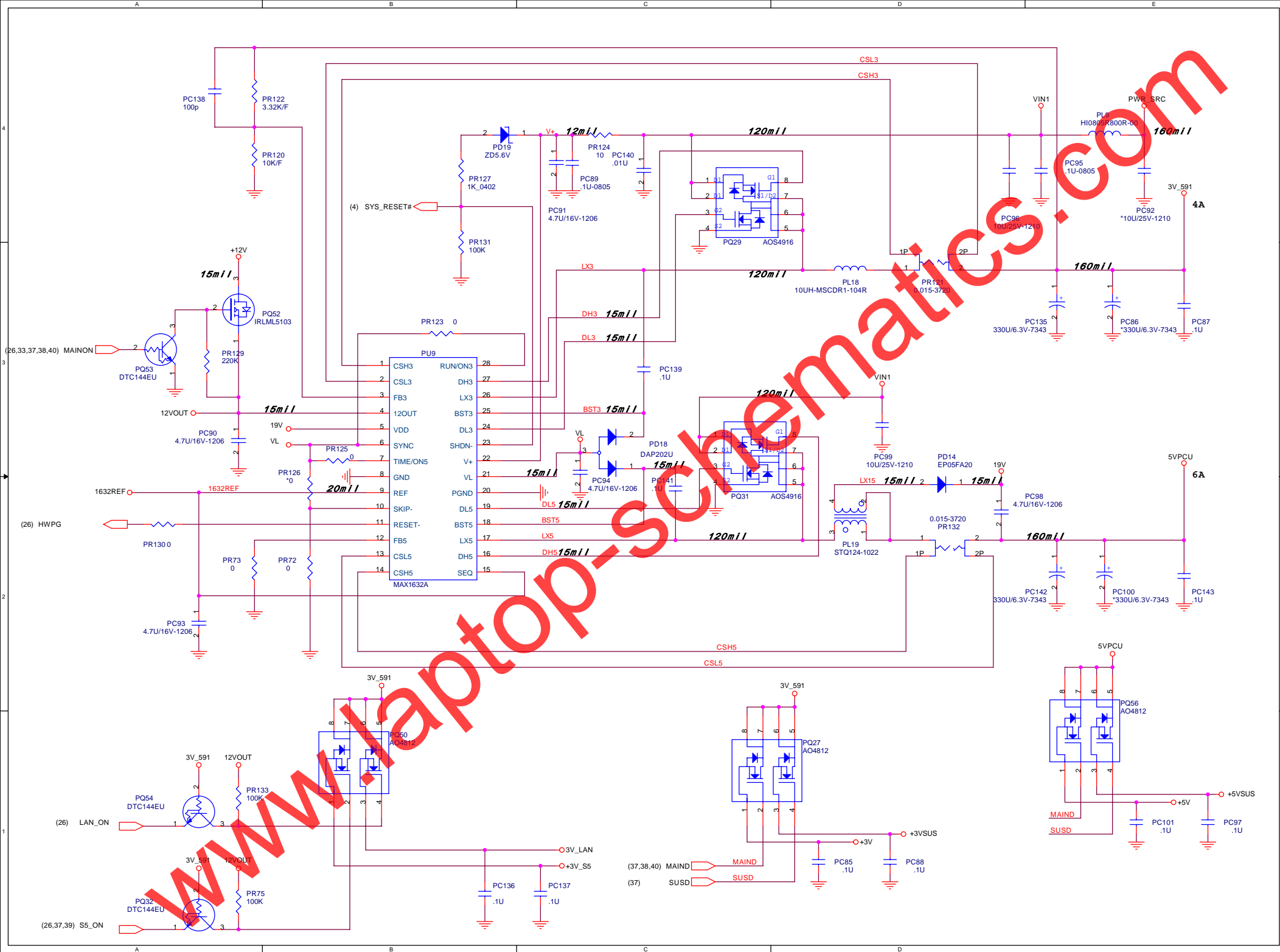
$L / RL(DCR) = Cqe * Rqe$

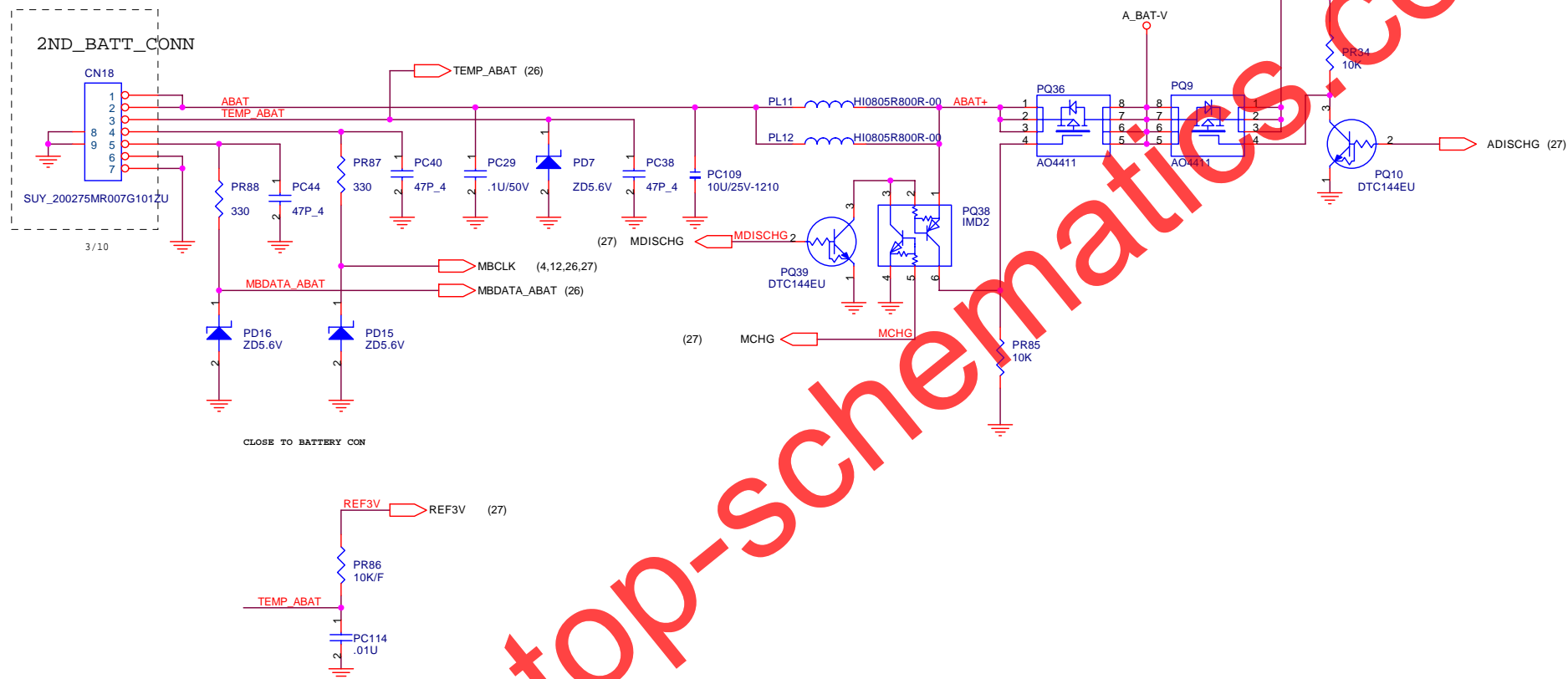
3R3 DCR = 0.0043
 $3.3u / 0.0043 = 0.1u * Rqe$
 $Rqe = 7.68K$

$L / RL(DCR) = Cqe * Rqe$

3R8 DCR = 0.0130
 $3.8u / 0.0130 = 0.1u * Rqe$
 $Rqe = 2.94K$



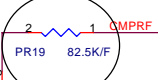




0714 PR19 change from

CS34223F901 42.2K/F to CS38253F909 82.5K/F

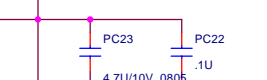
value provided
2.67% offset;
old value was
for old 4.62%
offset.



BG waveforms
improved. may
delete from
future
revision.

0714 PR27 change from

CS-33304JA09 3.3 to CS00004JA07 0



CHANGE CHOCK 0316



Set up for
constant-ripple
mode. Was
constant-frequency
mode

20 mil Trace list for layout

Added
filter for
PBOOT

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE
DH_VCORE2
LX_VCORE2
DL_VCORE2

10 mil Trace list for layout

SC1476
pin 4 pin
5 pin 7
pin 25
pin 30

0714 PC3 change from

CH31006K919 0.01u to CH31006K917 0.015u

0714 PR13 change from

CS32213F901 22.1K/F to CS33653F906 36.5K/F

0714 PR20 change from

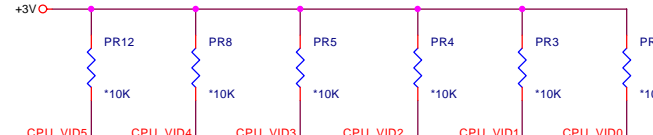
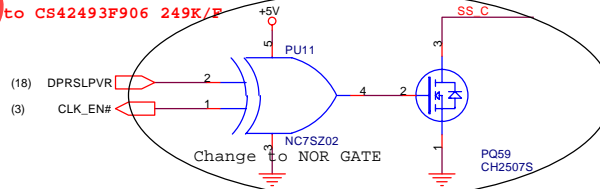
CS39003F909 20K/F to CS33323F901 33.2K/F

0714 PR23 change from

CS33323F901 33.2K/F to CS35493F902 54.9K/F

0714 PR11 change from

NC to CS42493F906 249K/F



0714 PR26 change from

CS17503F907 750/F to CS14753F905 475/F

0714 PR29 , PR21 change from

CS21543F901 1.54K/F to CS17153F905 715/F

0714 PC6 change from

CH16806J903 680p to CH12706J909 270p

0713 PC122 , PC66 change from

CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343